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RENESAS

MOS INTEGRATED CIRCUIT

MC-10118B

MULTIMEDIA PROCESSOR FOR MOBILE APPLICATIONS

DESCRIPTION

EMMA Mobile1-D512 (EM1-D512) (SIP: MC-10118B) is a multimedia processor for mobile applications that integrates a logic chip incorporating a CPU and DSP, and a Mobile DDR SDRAM chip, in one package.

As multimedia processor functions, EM1-D512 incorporates one CPU (ARM1176JZF-S™) and one DSP (SPXK701), achieving high-speed, power-efficient application processing. EM1-D512 also incorporates image processors with various functions to accelerate image processing.

Various power save modes enable the power to be controlled according to application processing. Moreover, power consumption can be reduced during standby by using sequences independent from the system.

FEATURES

- ○ CPU: ARM1176JZF-S (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
- ○ DSP: SPXK701 (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
- ○ Mobile DDR SDRAM (512Mb)
- ○ DMA controller: Memory ↔ memory and memory ↔ peripheral interface
- ○ Timers: General-purpose timers, watchdog timer (WDT)
- ○ Image processing
  - Image processor (resizing, filtering, etc.)
  - Image rotator (0°, 90°, 180°, 270°)
  - Graphics DMA (ROP and FILL)
  - Image composer (LCD output image synthesis)
- ○ H.264/MPEG-4 AVC accelerator application performance
  - H.264/MPEG-4 AVC Encode/Decode: D1 30 fps
- ○ Peripheral interfaces
  - Memory interface: External bus interface (16 bits: Flash memory, etc.), NAND interface
  - Serial interfaces: UART, I2C, audio/voice, SPI, IrDA
  - SD card interface
  - Image-related interfaces: LCD interface, terrestrial digital TV interface (DTV), ITU-R.BT656 interface (NTS), camera interface
  - General-purpose I/O interface
  - USB interface
- ○ Power supply voltage
  - Core power supply : V (1.2 V system : 1.1V - 1.3V)
  - IO power supply : VIO18 (1.8 V system : 1.7V - 1.9V), VIO3 (3 V system : 2.7V - 3.6V)

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Printed in Japan

Order Information

Order name	Package
MC-10118BF1-ENY-A	481-pin FPBGA (12.7mm×12.7mm)

RELATED DOCUMENTS

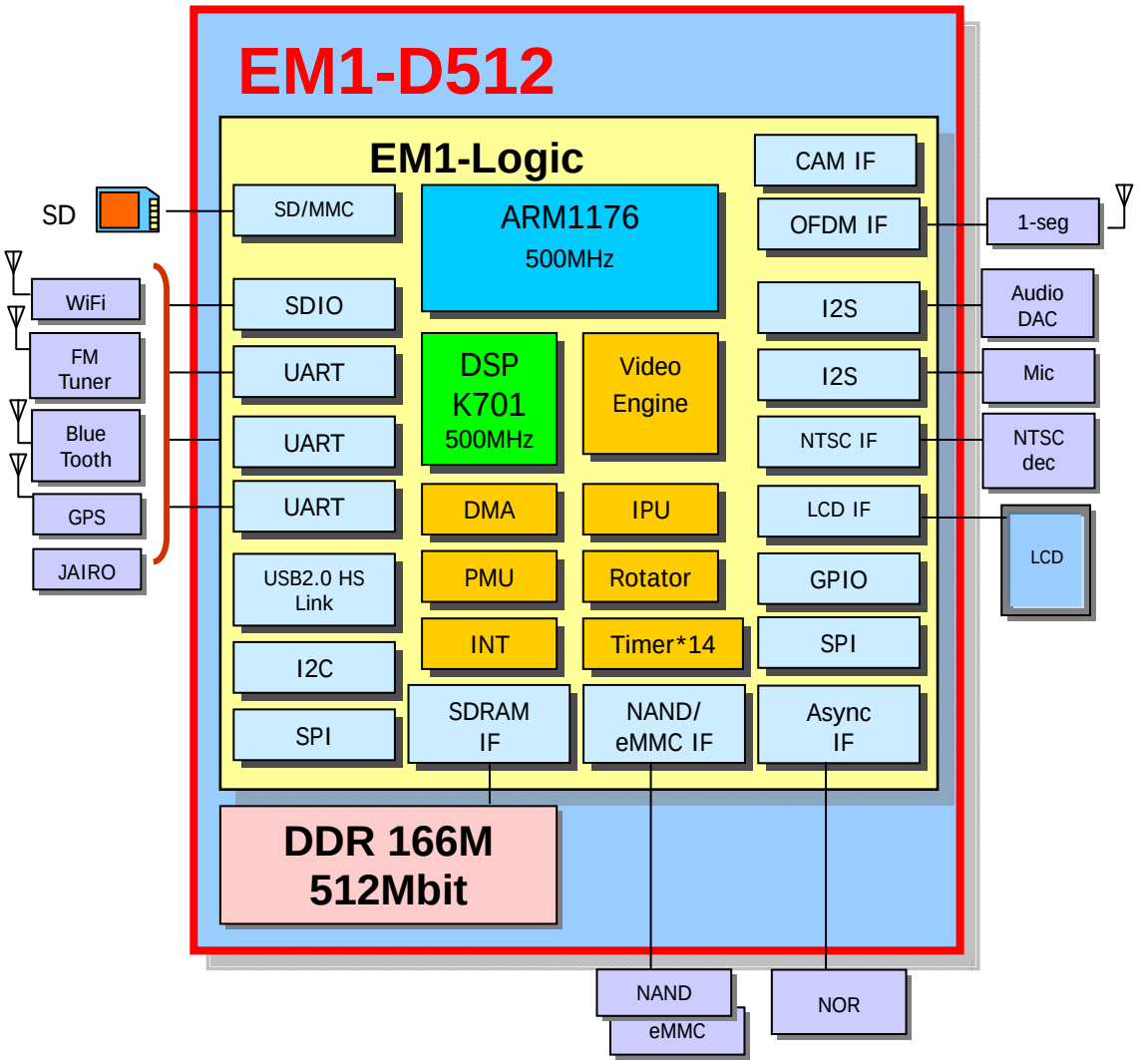
The functions of the multimedia processor for mobile applications are described in the following documents. Refer to these documents together with this data sheet during design operations.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- Multimedia Processor for Mobile Applications User's Manual
  - Audio/Voice and PWM Interfaces (R19UH0027EJ)
  - DDR SDRAM Interface (R19UH0028EJ)
  - DMA Controller (S19255E)
  - I2C Interface (S19256E)
  - ITU-R BT.656 Interface (S19257E)
  - LCD Controller (S19258E)
  - MICROWIRE (S19259E)
  - NAND Flash Interface (S19260E)
  - SPI (S19261E)
  - UART Interface (S19262E)
  - Image Composer (S19263E)
  - Image Processor Unit (S19264E)
  - System Control/General-Purpose I/O Interface (R19UH0029EJ)
  - Timer (S19266E)
  - Terrestrial Digital TV Interface (S19267E)
  - Camera Interface (S19285E)
  - USB Interface (S19359E)
  - SD Memory Card Interface (S19361E)
  - PDMA (S19373E)
  - One Chip (R19UH0030EJ)

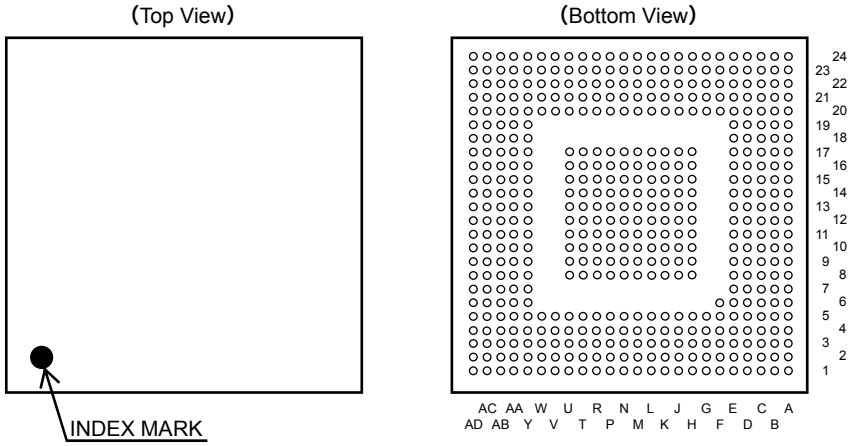
Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

BLOCK DIAGRAM



PIN LAYOUT

481-pin fine-pitch BGA package (12.7 × 12.7 mm)



Pin Assignment

(1/5)

Pin No.	Type	Pin Name
A1	–	G
A2	–	G
A3	–	G
A4	D	PWM0
A5	D	URT0_SRIN
A6	–	G
A7	–	V
A8	C	PM0_CLK
A9	B	C32K
A10	–	VA2
A11	–	G
A12	–	VA3
A13	–	V
A14	–	VIO3
A15	–	G
A16	D	REFCLKO
A17	Z	OSC12M_CKO
A18	Z	OSC12M_CKI
A19	–	G
A20	–	V
A21	–	VIO18
A22	–	G
A23	–	G
A24	–	G
B1	–	G
B2	–	G
B3	D	URT2_SOUT
B4	D	PWM1
B5	D	URT0_SOUT
B6	–	G
B7	–	V
B8	D	SP0_CLK
B9	C	IIC2_SDA
B10	–	VA2
B11	–	G
B12	–	VA3
B13	–	V
B14	–	VIO3
B15	–	G
B16	D	JT0_TMS
B17	A	DET1
B18	J	LCD_HSYNC
B19	–	G
B20	–	V
B21	–	VIO18
B22	J	LCD_G1
B23	–	G
B24	–	G
C1	–	G
C2	D	DTV_DATA
C3	D	URT2_SRIN
C4	D	URT2_RTSB
C5	D	URT0_RTSB
C6	–	G
C7	–	VIO3
C8	D	SP0_SI
C9	C	IIC2_SCL
C10	C	IIC_SDA
C11	–	VA1
C12	E	BOOTSEL1
C13	D	GIO_P2
C14	–	VIO3
C15	–	G
C16	D	JT0_TDI
C17	D	JT0_RTCK
C18	J	LCD_VSYNC
C19	J	LCD_B3
C20	J	LCD_B0
C21	J	LCD_G3
C22	J	LCD_G2
C23	J	LCD_G0
C24	–	G
D1	C	DTV_BCLK
D2	D	DTV_PSYNC
D3	D	DTV_VLD
D4	D	URT2_CTSB
D5	D	URT0_CTSB
D6	–	G
D7	–	VIO3
D8	D	SP0_SO
D9	D	PM0_SEN
D10	C	IIC_SCL
D11	–	VA1
D12	E	BOOTSEL2
D13	D	GIO_P3
D14	–	VIO3
D15	–	G
D16	D	JT0_TDO
D17	C	JT0_TRSTB
D18	J	LCD_ENABLE
D19	J	LCD_B4
D20	J	LCD_B1
D21	J	LCD_G4
D22	J	LCD_R5
D23	J	LCD_R4
D24	J	LCD_PXCLK
E1	–	V
E2	–	V
E3	–	VIO18
E4	–	VIO18
E5	D	GIO_P6
E6	D	GIO_P5
E7	D	GIO_P4
E8	D	SP0_CS2
E9	D	SP0_CS0
E10	D	PM0_SI
E11	R	TE2
E12	E	BOOTSEL3
E13	E	BOOTSEL0
E14	D	GIO_P0
E15	–	G
E16	C	JT0_TCK
E17	N	TESTRSTB
E18	M	TRSTB

(2/5)

Pin No.	Type	Pin Name
E19	J	LCD_B5
E20	J	LCD_B2
E21	J	LCD_G5
E22	J	LCD_R3
E23	J	LCD_R2
E24	J	LCD_R1
F1	–	G
F2	–	G
F3	–	G
F4	–	G
F5	D	GIO_P7
F6	–	G
F20	J	LCD_R0
F21	M	AB0_CSB3
F22	M	AB0_CSB2
F23	–	V
F24	–	V
G1	–	VDDQ_DDR
G2	–	VDDQ_DDR
G3	–	VDD_DDR
G4	–	VDD_DDR
G5	D	GIO_P8
G20	M	AB0_CSB1
G21	–	G
G22	–	G
G23	–	G
G24	–	G
H1	C	NTS_CLK
H2	D	NTS_VS
H3	D	NTS_HS
H4	D	NTS_DATA0
H5	D	NTS_DATA5
H8	D	SP0_CS1
H9	D	PM0_SO
H10	D	ERR_RST_REQB
H11	–	G
H12	Q	TE1
H13	C	A_RESETB

Pin No.	Type	Pin Name
H14	D	GIO_P1
H15	–	G
H16	J	DEBUG_EN
H17	E	UTEST
H20	M	AB0_CSB0
H21	–	VDD_DDR
H22	–	VDD_DDR
H23	–	VDD_DDR
H24	–	VDD_DDR
J1	D	NTS_DATA1
J2	D	NTS_DATA2
J3	D	NTS_DATA3
J4	D	NTS_DATA4
J5	D	NTS_DATA6
J8	–	G
J9	–	G
J10	–	G
J11	–	G
J12	–	G
J13	–	G
J14	–	G
J15	–	G
J16	–	G
J17	–	G
J20	M	AB0_WAIT
J21	M	AB0_BEN1
J22	M	AB0_BEN0
J23	M	AB0_A26
J24	M	AB0_A25
K1	C	SD1_CKI
K2	D	SD1_CMD
K3	D	SD1_CKO
K4	D	SD1_DATA0
K5	D	NTS_DATA7
K8	–	G
K9	–	G
K10	–	G
K11	–	G

Pin No.	Type	Pin Name
K12	–	G
K13	–	G
K14	–	G
K15	–	G
K16	–	G
K17	–	IC
K20	M	AB0_A24
K21	M	AB0_A23
K22	M	AB0_A22
K23	M	AB0_A21
K24	M	AB0_A20
L1	D	SD1_DATA1
L2	D	SD1_DATA2
L3	D	SD1_DATA3
L4	D	SD0_CMD
L5	D	SD0_DATA0
L8	–	G
L9	–	G
L10	–	G
L11	–	G
L12	–	G
L13	–	G
L14	–	G
L15	–	G
L16	–	G
L17	–	G
L20	M	AB0_A19
L21	–	V
L22	–	V
L23	–	VIO18
L24	–	VIO18
M1	–	VIO3
M2	–	VIO3
M3	–	VIO3
M4	–	VIO3
M5	D	SD0_DATA1
M8	–	G
M9	–	G

Remark IC : Internally-connected pins (Leave open)

(3/5)

Pin No.	Type	Pin Name
M10	–	G
M11	–	G
M12	–	G
M13	–	G
M14	–	G
M15	–	G
M16	–	G
M17	–	G
M20	M	AB0_A18
M21	–	G
M22	–	G
M23	–	G
M24	–	G
N1	–	G
N2	–	G
N3	–	G
N4	–	G
N5	–	G
N8	–	G
N9	–	G
N10	–	G
N11	–	G
N12	–	G
N13	–	G
N14	–	G
N15	–	G
N16	–	G
N17	–	G
N20	M	AB0_A17
N21	–	VDD_DDR
N22	–	VDD_DDR
N23	–	VDD_DDR
N24	–	VDD_DDR
P1	–	VDD_DDR
P2	–	VDD_DDR
P3	–	VDDQ_DDR
P4	–	VDDQ_DDR
P5	–	VDDQ_DDR

Pin No.	Type	Pin Name
P8	–	G
P9	–	G
P10	–	G
P11	–	G
P12	–	G
P13	–	G
P14	–	G
P15	–	G
P16	–	G
P17	–	G
P20	M	AB0_WRB
P21	M	AB0_RDB
P22	P	AB0_AD15
P23	P	AB0_AD14
P24	P	AB0_AD13
R1	C	SD0_CKI
R2	D	SD0_DATA2
R3	D	SD0_DATA3
R4	D	SD2_CMD
R5	D	GIO_P9
R8	–	G
R9	–	G
R10	–	G
R11	–	G
R12	–	G
R13	–	G
R14	–	G
R15	–	G
R16	–	G
R17	–	G
R20	P	AB0_AD12
R21	P	AB0_AD11
R22	P	AB0_AD10
R23	P	AB0_AD9
R24	J	AB0_CLK
T1	D	SD0_CKO
T2	D	SD2_DATA0
T3	D	SD2_DATA1

Pin No.	Type	Pin Name
T4	D	SD2_DATA2
T5	D	GIO_P10
T8	–	G
T9	–	G
T10	–	G
T11	–	G
T12	–	IC
T13	–	IC
T14	–	G
T15	–	G
T16	–	G
T17	–	G
T20	P	AB0_AD8
T21	P	AB0_AD7
T22	P	AB0_AD6
T23	P	AB0_AD5
T24	P	AB0_AD4
U1	–	V
U2	–	V
U3	–	V
U4	–	V
U5	–	V
U8	–	G
U9	–	G
U10	–	G
U11	–	G
U12	–	IC
U13	–	IC
U14	–	IC
U15	–	IC
U16	–	IC
U17	–	G
U20	P	AB0_AD3
U21	–	V
U22	–	V
U23	–	VIO18
U24	–	VIO18
V1	–	G

Remark IC : Internally-connected pins (Leave open)

(4/5)

Pin No.	Type	Pin Name
V2	–	G
V3	–	G
V4	–	G
V5	–	G
V20	P	AB0_AD2
V21	–	G
V22	–	G
V23	–	G
V24	–	G
W1	–	VDDQ_DDR
W2	–	VDDQ_DDR
W3	–	VDD_DDR
W4	–	VDD_DDR
W5	–	IC
W20	P	AB0_AD1
W21	–	VDD_DDR
W22	–	VDD_DDR
W23	–	VDD_DDR
W24	–	VDD_DDR
Y1	–	VIO3
Y2	–	VIO3
Y3	–	VIO3
Y4	–	VIO3
Y5	–	IC
Y6	–	IC
Y7	–	IC
Y8	–	IC
Y9	–	IC
Y10	–	IC
Y11	–	V
Y12	–	IC
Y13	–	IC
Y14	–	IC
Y15	–	IC
Y16	–	IC
Y17	–	IC
Y18	–	IC
Y19	–	IC
Y20	–	IC

Pin No.	Type	Pin Name
Y21	P	AB0_AD0
Y22	G	AB0_ADV
Y23	G	USB_STP
Y24	G	USB_CLK
AA1	C	SD2_CKI
AA2	D	SD2_DATA3
AA3	–	IC
AA4	–	IC
AA5	–	IC
AA6	–	G
AA7	–	IC
AA8	–	IC
AA9	–	IC
AA10	–	G
AA11	–	V
AA12	–	IC
AA13	–	IC
AA14	–	IC
AA15	–	G
AA16	–	IC
AA17	–	IC
AA18	–	VIO18
AA19	–	G
AA20	–	IC
AA21	G	USB_DATA7
AA22	G	USB_DATA6
AA23	G	USB_DATA5
AA24	G	USB_NXT
AB1	–	G
AB2	D	SD2_CKO
AB3	–	IC
AB4	–	IC
AB5	–	IC
AB6	–	G
AB7	–	VIO18
AB8	–	IC
AB9	–	IC
AB10	–	G
AB11	–	VIO18

Pin No.	Type	Pin Name
AB12	–	IC
AB13	–	IC
AB14	–	IC
AB15	–	G
AB16	–	IC
AB17	–	IC
AB18	–	VIO18
AB19	–	G
AB20	–	IC
AB21	G	USB_DATA4
AB22	G	USB_DIR
AB23	G	USB_DATA3
AB24	–	G
AC1	–	G
AC2	–	G
AC3	–	IC
AC4	–	IC
AC5	–	V
AC6	–	G
AC7	–	VIO18
AC8	–	IC
AC9	–	IC
AC10	–	G
AC11	–	VIO18
AC12	–	IC
AC13	–	IC
AC14	–	IC
AC15	–	G
AC16	–	IC
AC17	–	IC
AC18	–	V
AC19	–	G
AC20	–	IC
AC21	G	USB_DATA1
AC22	G	USB_DATA2
AC23	–	G
AC24	–	G
AD1	–	G
AD2	–	G

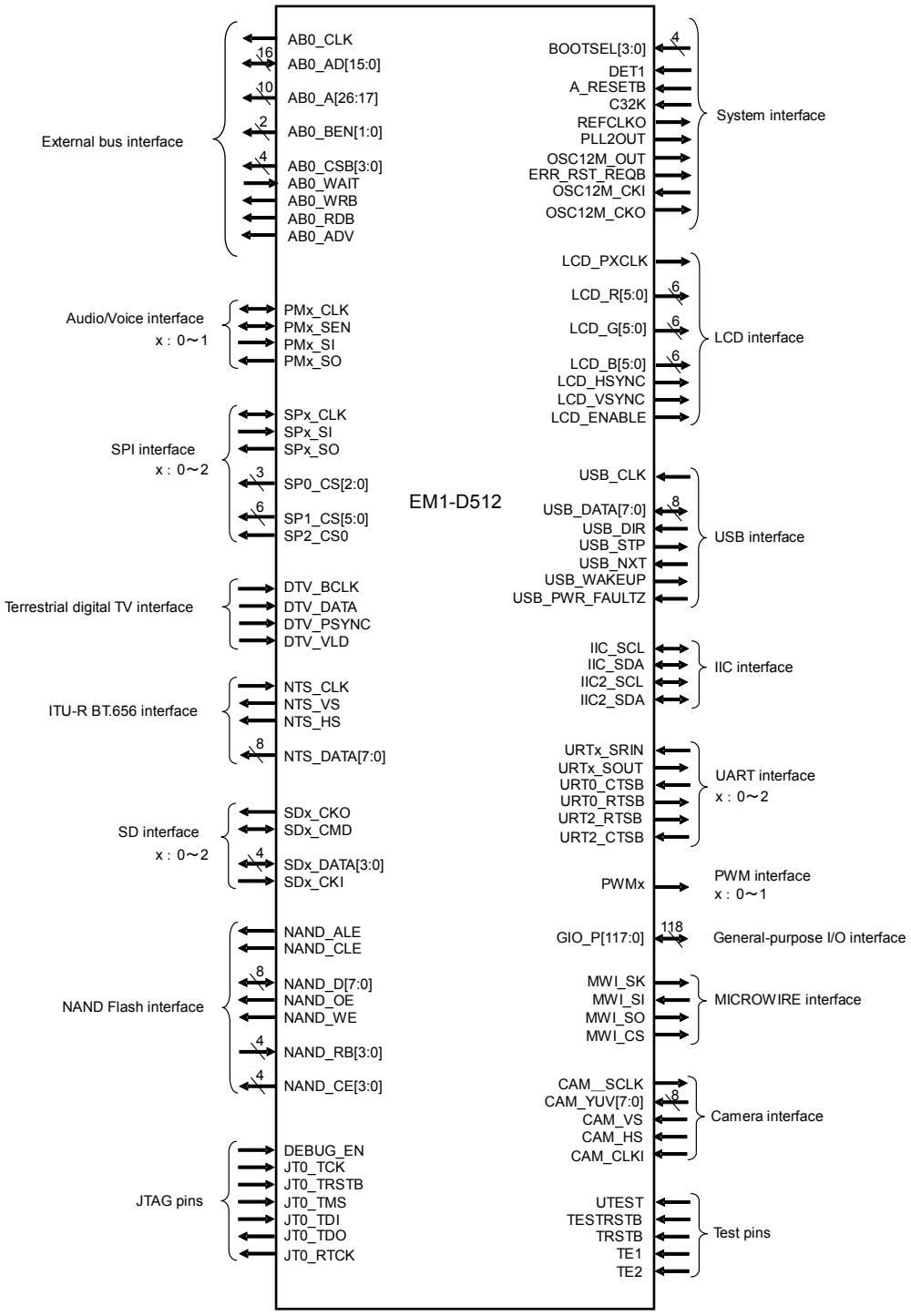
(5/5)

Pin No.	Type	Pin Name
AD3	–	G
AD4	–	IC
AD5	–	V
AD6	–	G
AD7	–	VIO18
AD8	–	IC
AD9	–	IC
AD10	–	G
AD11	–	VIO18
AD12	–	IC
AD13	–	IC
AD14	–	IC
AD15	–	G
AD16	–	IC
AD17	–	IC
AD18	–	V
AD19	–	G
AD20	–	IC
AD21	G	USB_DATA0
AD22	–	G
AD23	–	G
AD24	–	G

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Configuration



1.2 Pin Functions

(1) Boot select signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
BOOTSEL3	E12	Input	Boot mode selection 3	–	E	–
BOOTSEL2	D12	Input	Boot mode selection 2	–	E	–
BOOTSEL1	C12	Input	Boot mode selection 1	–	E	–
BOOTSEL0	E13	Input	Boot mode selection 0	–	E	–

(2) System control signals (VIO3 / VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DET1	B17	Input	Power-on reset	–	A	–
A_RESETB	H13	Input	System reset	–	C	–.
C32K	A9	Input	Reference clock (32.768 kHz)	–	B	–.
REFCLKO	A16	Output	Reference clock	PLL2OUT OSC12M_OUT	D	Leave open.
PLL2OUT	A16	Output	Internal PLL2 output	REFCLKO OSC12M_OUT	D	Leave open.
OSC12M_OUT	A16	Output	Internal OSC output	REFCLKO PLL2OUT	D	Leave open.
ERR_RST_REQB	H10	Output	Error reset request	–	D	Leave open.
OSC12M_CKI NOTE	A18	Input	OSC XT1	–	Z	Leave open.
OSC12M_CKO NOTE	A17	Output	OSC XT2	–	Z	Leave open.

Note VIO18

(3) External bus interface signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
AB0_CLK	R24	Output	Clock	GIO_P11 NTS_CLK	J	Leave open.
AB0_AD[15:0]	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	Data	GIO_P[27:12]	P	Leave open.
AB0_A[26:20]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[10:4]	M	Leave open.
AB0_A[19:17]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
AB0_A[10:4]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[26:20]	M	Leave open
AB0_A[3:1]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[19:17]	M	Leave open
AB0_BEN[1:0]	J21, J22	Output	Byte enable	GIO_P[47:46]	M	Leave open.
AB0_CSB3	F21	Output	Chip select	GIO_P45 NTS_HS	M	Leave open.
AB0_CSB2	F22	Output	Chip select	GIO_P44 NTS_VS	M	Leave open.
AB0_CSB1	G20	Output	Chip select	GIO_P43 NTS_DATA7	M	Leave open.
AB0_CSB0	H20	Output	Chip select	GIO_P42 NTS_DATA6	M	Leave open.
AB0_WAIT	J20	Input	Wait	GIO_P41 NTS_DATA5	M	Leave open.
AB0_WRB	P20	Output	Write strobe	GIO_P40 NTS_DATA4	M	Leave open.
AB0_RDB	P21	Output	Read strobe	GIO_P39 NTS_DATA3	M	Leave open.
AB0_ADV	Y22	Output	Address enable	GIO_P38	G	Leave open.

(4) Audio interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PM0_CLK	A8	I/O	PCM0 clock (default input)	–	C	Leave open.
PM0_SEN	D9	I/O	PCM0 frame synchronization (default input)	–	D	Leave open.
PM0_SI	E10	Input	PCM0 data	GIO_P87	D	Leave open.
PM0_SO	H9	Output	PCM0 data	–	D	Leave open.
PM1_CLK	H1	I/O	PCM1 clock (default input)	GIO_P72 NTS_CLK	C	Leave open.
PM1_SEN	H5	I/O	PCM1 frame synchronization (default input)	GIO_P80 NTS_DATA5 SP1_CS4	D	Leave open.
PM1_SI	J5	Input	PCM1 data	GIO_P81 NTS_DATA6 SP1_CS5	D	Leave open.
PM1_SO	K5	Output	PCM1 data	GIO_P82 NTS_DATA7	D	Leave open.

(5) Camera interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
CAM_SCLK	E6	Output	Camera clock	GIO_P5, NAND_RB2	D	Leave open.
CAM_CLKI	K1	Input	Camera interface	GIO_P92, SD1_CKI	C	Leave open.
CAM_YUV7	L1	Input	Camera interface	SD1_DATA1	D	Leave open.
CAM_YUV6	K4	Input	Camera interface	SD1_DATA0	D	Leave open.
CAM_YUV5	K2	Input	Camera interface	SD1_CMD	D	Leave open.
CAM_YUV4	J4	Input	Camera interface	NTS_DATA4, SP1_CS3 GIO_P79	D	Leave open.
CAM_YUV3	J3	Input	Camera interface	NTS_DATA3, SP1_CS2 GIO_P78	D	Leave open.
CAM_YUV2	J2	Input	Camera interface	NTS_DATA2, SP1_CS1 GIO_P77	D	Leave open.
CAM_YUV1	J1	Input	Camera interface	NTS_DATA1, SP1_CS0 GIO_P76	D	Leave open
CAM_YUV0	H4	Input	Camera interface	NTS_DATA0, SP1_SO GIO_P75	D	Leave open
CAM_HS	L3	Input	Camera interface	SD1_DATA3	D	Leave open
CAM_VS	L2	Input	Camera interface	SD1_DATA2	D	Leave open

(6) SPI interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SP0_CLK	B8	I/O	SPI0 clock output	MWI_SK	D	Leave open.
SP0_SI	C8	Input	SPI0 data	MWI_SI	D	Leave open.
SP0_SO	D8	Output	SPI0 data	MWI_SO	D	Leave open.
SP0_CS0	E9	I/O	SPI0 chip select	MWI_CS	D	Leave open.
SP0_CS[2:1]	E8, H8	Output	SPI0 chip select	GIO_P[49:48]	D	Leave open.
SP1_CLK	H2	I/O	SPI1 clock input	GIO_P73 NTS_VS	D	Leave open.
SP1_SI	H3	Input	SPI1 data	GIO_P74 NTS_HS	D	Leave open.
SP1_SO	H4	Output	SPI1 data	GIO_P75 NTS_DATA0 CAM_YUV0	D	Leave open.
SP1_CS5	J5	Output	SPI1 chip select	GIO_P81 NTS_DATA6 PM1_SI	D	Leave open.
SP1_CS4	H5	Output	SPI1 chip select	GIO_P80 NTS_DATA5 PM1_SEN	D	Leave open.
SP1_CS[3:1]	J4, J3, J2	Output	SPI1 chip select	GIO_P[79:77] NTS_DATA[4:2] CAM_YUV[4:2]	D	Leave open.
SP1_CS0	J1	I/O	SPI1 chip select	GIO_P76 NTS_DATA1 CAM_YUV1	D	Leave open.
SP2_CLK	D1	I/O	SPI2 clock input	DTV_BCLK	C	Leave open.
SP2_SI	C2	Input	SPI2 data	DTV_DATA	D	Leave open.
SP2_SO	D2	Output	SPI2 data	DTV_PSYNC	D	Leave open.
SP2_CS0	D3	I/O	SPI2 chip select	DTV_VLD	D	Leave open.

(7) Terrestrial digital TV interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DTV_BCLK	D1	Input	Clock	SP2_CLK	C	Leave open.
DTV_DATA	C2	Input	YUV data	SP2_SI	D	Leave open.
DTV_PSYNC	D2	Input	Vertical synchronization	SP2_SO	D	Leave open.
DTV_VLD	D3	Input	Horizontal synchronization	SP2_CS0	D	Leave open.

(8) LCD interface signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
LCD_PXCLK	D24	Output	Pixel clock	GIO_P50	J	Leave open.
LCD_R[5:0]	D22, D23, E22, E23, E24, F20	Output	Red data	GIO_P[56:51]	J	Leave open.
LCD_G[5:0]	E21, D21, C21, C22, B22, C23	Output	Green data	GIO_P[62:57]	J	Leave open.
LCD_B[5:0]	E19, D19, C19, E20, D20, C20	Output	Blue data	GIO_P[68:63]	J	Leave open.
LCD_HSYNC	B18	Output	Horizontal synchronization	GIO_P69	J	Leave open.
LCD_VSYNC	C18	Output	Vertical synchronization	GIO_P70	J	Leave open.
LCD_ENABLE	D18	Output	Data enable	GIO_P71	J	Leave open.

(9) USB interface signals (VIO18 / VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
USB_CLK	Y24	Input	Clock	GIO_P96	G	Leave open.
USB_DATA[7:0]	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	USB data	GIO_P[104:97]	G	Leave open.
USB_DIR	AB22	Input	USB DIR input	GIO_P105	G	Leave open.
USB_STP	Y23	Output	USB STOP output	GIO_P106	G	Leave open.
USB_NXT	AA24	Input	USB NXT input	GIO_P107	G	Leave open.
USB_WAKEUP NOTE	H14	Output	Suspend wakeup	GIO_P1 USB_PWR_FAULT	D	Leave open.
USB_PWR_FAULT NOTE	H14	Input	Power fault	GIO_P1 USB_WAKEUP	D	Leave open.

Note VIO3

(10) ITU-R BT.656 interface signals (VIO3 / VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
NTS_CLK	H1	Input	Clock	GIO_P72, PM1_CLK	C	Leave open.
	R24 Note			AB0_CLK, GIO_P11	J	Leave open
NTS_VS	H2	Output	Vertical synchronization	GIO_P73, SP1_CLK	D	Leave open.
	F22 Note			AB0_CSB2, GIO_P44	M	Leave open.
NTS_HS	H3	Output	Horizontal synchronization	GIO_P74, SP1_SI	D	Leave open.
	F21 Note			AB0_CSB3, GIO_P45	M	Leave open.
NTS_DATA7	K5	Output	NTSC data	GIO_P82, PM1_SO	D	Leave open.
	G20 Note			AB0_CSB1, GIO_P43	M	Leave open
NTS_DATA6	J5	Output	NTSC data	GIO_P81, SP1_CS5 PM1_SI	D	Leave open.
	H20 Note			AB0_CSB0, GIO_P42	M	Leave ope
NTS_DATA5	H5	Output	NTSC data	GIO_P80, SP1_CS4 PM1_SEN	D	Leave open.
	J20 Note			AB0_WAIT, GIO_P41	M	Leave open.
NTS_DATA4	J4	Output	NTSC data	GIO_P79, SP1_CS3 CAM_YUV4	D	Leave open.
	P20 Note			AB0_WRB, GIO_P40	M	Leave open.
NTS_DATA3	J3	Output	NTSC data	GIO_P78, SP1_CS2 CAM_YUV3	D	Leave open.
	P21 Note			AB0_RDB, GIO_P39	M	Leave open
NTS_DATA2	J2	Output	NTSC data	GIO_P77, SP1_CS1 CAM_YUV2	D	Leave open.
	L20 Note			AB0_A3, AB0_A19, GIO_P30	M	Leave open
NTS_DATA1	J1	Output	NTSC data	GIO_P76, SP1_CS0 CAM_YUV1	D	Leave open.
	M20 Note			AB0_A2, AB0_A18, GIO_P29	M	Leave ope
NTS_DATA0	H4	Output	NTSC data	GIO_P75, SPI_SO CAM_YUV0	D	Leave open.
	N20 Note			AB0_A1, AB0_A17, GIO_P28	M	Leave open.

Note VIO18

(11) IIC interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
IIC_SCL	D10	Output	Serial clock input	GIO_P83	C	Leave open.
IIC_SDA	C10	I/O	Serial data input	GIO_P84	C	Leave open.
IIC2_SCL	C9	Output	Serial clock input	NAND_WE	C	Leave open.
IIC2_SDA	B9	I/O	Serial data input	NAND_RB0	C	Leave open.

(12) UART interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
URT0_SRIN	A5	Input	Serial data	–	D	Leave open.
URT0_SOUT	B5	Output	Serial data	–	D	Leave open.
URT0_CTSB	D5	Input	Data transmission/reception ready in destination device	GIO_P85 URT1_SRIN	D	Leave open.
URT0_RTSB	C5	Output	Data transmission/reception ready	GIO_P86 URT1_SOUT	D	Leave open.
URT1_SRIN	D5	Input	Serial data	GIO_P85 URT0_CTSB	D	Leave open.
URT1_SOUT	C5	Output	Serial data	GIO_P86 URT0_RTSB	D	Leave open.
URT2_SRIN	C3	Input	Serial data	GIO_P108 NAND_ALE	D	Leave open.
URT2_SOUT	B3	Output	Serial data	GIO_P109 NAND_CLE	D	Leave open.
URT2_CTSB	D4	Input	Data transmission/reception ready in destination device	GIO_P110 NAND_D0	D	Leave open.
URT2_RTSB	C4	Output	Data transmission/reception ready	GIO_P111 NAND_D1	D	Leave open.

(13) Memory card interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SD0_CKO	T1	Output	Clock	–	D	Leave open.
SD0_CMD	L4	I/O	Command response	–	D	Leave open.
SD0_DATA[3:1]	R3, R2, M5	I/O	Data	GIO_P[90:88]	D	Leave open.
SD0_DATA0	L5	I/O	Data	–	D	Leave open.
SD0_CKI	R1	Input	Loop back	GIO_P91	C	Leave open.
SD1_CKO	K3	Output	Clock	–	D	Leave open.
SD1_CMD	K2	I/O	Command response	CAM_YUV5	D	Leave open.
SD1_DATA3	L3	I/O	Data	CAM_HS	D	Leave open.
SD1_DATA2	L2	I/O	Data	CAM_VS	D	Leave open.
SD1_DATA1	L1	I/O	Data	CAM_YUV7	D	Leave open.
SD1_DATA0	K4	I/O	Data	CAM_YUV6	D	Leave open.
SD1_CKI	K1	Input	Loop back	GIO_P92 CAM_CLKI	C	Leave open.
SD2_CKO	AB2	Output	Clock	GIO_P112 NAND_D2	D	Leave open.
SD2_CMD	R4	I/O	Command response	GIO_P113 NAND_D3	D	Leave open.
SD2_DATA[3:0]	AA2, T4, T3, T2	I/O	Data	GIO_P[117:114] NAND_D[7:4]	D	Leave open.
SD2_CKI	AA1	Input	Loop back	GPIO_P93 NAND_OE	C	Leave open.

(14) PWM interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PWM0	A4	Output	PWM output	GIO_P94	D	Leave open.
PWM1	B4	Output	PWM output	GIO_P95	D	Leave open.

(15) General-purpose I/O interface signals (VIO18 / VIO3)

(1/3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P[117:114]	AA2, T4, T3, T2	I/O	General-purpose IO	SD2_DATA[3:0] NAND_D[7:4]	D	Leave open.
GIO_P113	R4	I/O	General-purpose IO	SD2_CMD NAND_D3	D	Leave open.
GIO_P112	AB2	I/O	General-purpose IO	SD2_CKO NAND_D2	D	Leave open.
GIO_P111	C4	I/O	General-purpose IO	URT2_RTSB NAND_D1	D	Leave open.
GIO_P110	D4	I/O	General-purpose IO	URT2_CTSB NAND_D0	D	Leave open.
GIO_P109	B3	I/O	General-purpose IO	URT2_SOUT NAND_CLE	D	Leave open.
GIO_P108	C3	I/O	General-purpose IO	URT2_SRIN NAND_ALE	D	Leave open.
GIO_P107 Note	AA24	I/O	General-purpose IO	USB_NXT	G	Leave open.
GIO_P106 Note	Y23	I/O	General-purpose IO	USB_STP	G	Leave open.
GIO_P105 Note	AB22	I/O	General-purpose IO	USB_DIR	G	Leave open.
GIO_P[104:97] Note	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	General-purpose IO	USB_DATA[7:0]	G	Leave open.
GIO_P96 Note	Y24	I/O	General-purpose IO	USB_CLK	G	Leave open.
GIO_P[95:94]	B4, A4	I/O	General-purpose IO	PWM[1:0]	D	Leave open.
GIO_P93	AA1	I/O	General-purpose IO	SD2_CKI NAND_OE	C	Leave open.
GIO_P92	K1	I/O	General-purpose IO	SD1_CKI CAM_CLKI	C	Leave open.
GIO_P91	R1	I/O	General-purpose IO	SD0_CKI	C	Leave open.
GIO_P[90:88]	R3, R2, M5	I/O	General-purpose IO	SD0_DATA[3:1]	D	Leave open.
GIO_P87	E10	I/O	General-purpose IO	PM0_SI	D	Leave open.
GIO_P86	C5	I/O	General-purpose IO	URT0_RTSB URT1_SOUT	D	Leave open.
GIO_P85	D5	I/O	General-purpose IO	URT0_CTSB URT1_SRIN	D	Leave open.
GIO_P84	C10	I/O	General-purpose IO	IIC_SDA	C	Leave open.
GIO_P83	D10	I/O	General-purpose IO	IIC_SCL	C	Leave open.

(2/3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P82	K5	I/O	General-purpose IO	NTS_DATA7 PM1_SO	D	Leave open.
GIO_P81	J5	I/O	General-purpose IO	NTS_DATA6 SP1_CS5 PM1_SI	D	Leave open.
GIO_P80	H5	I/O	General-purpose IO	NTS_DATA5 SP1_CS4 PM1_SEN	D	Leave open.
GIO_P[79:76]	J4, J3, J2, J1	I/O	General-purpose IO	NTS_DATA[4:1] SP1_CS[3:0] CAM_YUV[4:1]	D	Leave open.
GIO_P75	H4	I/O	General-purpose IO	NTS_DATA0 SP1_SO CAM_YUV0	D	Leave open.
GIO_P74	H3	I/O	General-purpose IO	NTS_HS SP1_SI	D	Leave open.
GIO_P73	H2	I/O	General-purpose IO	NTS_VS SP1_CLK	D	Leave open.
GIO_P72	H1	I/O	General-purpose IO	NTS_CLK PM1_CLK	C	Leave open.
GIO_P71 Note	D18	I/O	General-purpose IO	LCD_ENABLE	J	Leave open.
GIO_P70 Note	C18	I/O	General-purpose IO	LCD_VSYNC	J	Leave open.
GIO_P69 Note	B18	I/O	General-purpose IO	LCD_HSYNC	J	Leave open.
GIO_P[68:63] Note	E19, D19, C19, E20, D20, C20	I/O	General-purpose IO	LCD_B[5:0]	J	Leave open.
GIO_P[62:57] Note	E21, D21, C21, C22, B22, C23	I/O	General-purpose IO	LCD_G[5:0]	J	Leave open.
GIO_P[56:51] Note	D22, D23, E22, E23, E24, F20	I/O	General-purpose IO	LCD_R[5:0]	J	Leave open.
GIO_P50 Note	D24	I/O	General-purpose IO	LCD_PXCLK	J	Leave open.
GIO_P[49:48] Note	E8, H8	I/O	General-purpose IO	SP0_CS[2:1]	D	Leave open.
GIO_P[47:46] Note	J21,J22	I/O	General-purpose IO	AB0_BEN[1:0]	M	Leave open.
GIO_P45 Note	F21	I/O	General-purpose IO	AB0_CSB3 NTS_HS	M	Leave open.
GIO_P44 Note	F22	I/O	General-purpose IO	AB0_CSB2 NTS_VS	M	Leave open.
GIO_P43 Note	G20	I/O	General-purpose IO	AB0_CSB1 NTS_DATA7	M	Leave open.
GIO_P42 Note	H20	I/O	General-purpose IO	AB0_CSB0 NTS_DATA6	M	Leave open.

(3/3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P41 Note	J20	I/O	General-purpose IO	AB0_WAIT NTS_DATA5	M	Leave open.
GIO_P40 Note	P20	I/O	General-purpose IO	AB0_WRB NTS_DATA4	M	Leave open.
GIO_P39 Note	P21	I/O	General-purpose IO	AB0_RDB NTS_DATA3	M	Leave open.
GIO_P38 Note	Y22	I/O	General-purpose IO	AB0_ADV	G	Leave open.
GIO_P[37:31] Note	J23, J24, K20, K21, K22, K23, K24	I/O	General-purpose IO	AB0_A[26:20] AB0_A[10:4]	M	Leave open.
GIO_P[30:28] Note	L20, M20, N20	I/O	General-purpose IO	AB0_A[19:17] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
GIO_P[27:12] Note	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	General-purpose IO	AB0_AD[15:0]	P	Leave open.
GIO_P11 Note	R24	I/O	General-purpose IO	AB0_CLK NTS_CLK	J	Leave open.
GIO_P[10:7]	T5, R5, G5, F5	I/O	General-purpose IO	NAND_CE[3:0]	D	Leave open.
GIO_P6	E5	I/O	General-purpose IO	NAND_RB3	D	Leave open.
GIO_P5	E6	I/O	General-purpose IO	NAND_RB2 CAM_SCLK	D	Leave open.
GIO_P4	E7	I/O	General-purpose IO	NAND_RB1	D	Leave open.
GIO_P[3:2]	D13, C13	I/O	General-purpose IO	–	D	Leave open.
GIO_P1	H14	I/O	General-purpose IO	USB_WAKEUP USB_PWR_FAULT	D	Leave open.
GIO_P0	E14	I/O	General-purpose IO	–	D	Leave open.

Note VIO18

(16) MICROWIRE interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
MWI_SK	B8	Output	Clock	SP0_CLK	D	Leave open.
MWI_SI	C8	Input	Data	SP0_SI	D	Leave open.
MWI_SO	D8	Output	Data	SP0_SO	D	Leave open.
MWI_CS	E9	Output	Chip select	SP0_CS0	D	Leave open.

(17) NAND Flash interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
NAND_ALE	C3	Output	Address latch enable	URT2_SRIN GIO_P108	D	Leave open.
NAND_CLE	B3	Output	Command latch enable	URT2_SOUT GIO_P109	D	Leave open.
NAND_D[7:4]	AA2, T4 T3, T2	I/O	Data	SD2_DATA[3:0] GIO_P[117:114]	D	Leave open.
NAND_D3	R4	I/O	Data	SD2_CMD GIO_P113	D	Leave open.
NAND_D2	AB2	I/O	Data	SD2_CKO GIO_P112	D	Leave open.
NAND_D1	C4	I/O	Data	URT2_RTSB GIO_P111	D	Leave open.
NAND_D0	D4	I/O	Data	URT2_CTSB GIO_P110	D	Leave open.
NAND_OE	AA1	Output	Output enable	SD2_CKI GIO_P93	C	Leave open.
NAND_WE	C9	Output	Write enable	IIC2_SCL	C	Leave open.
NAND_RB0	B9	Input	Ready busy	IIC2_SDA	C	Leave open.
NAND_RB3	E5	Input	Ready busy	GIO_P6	D	Leave open.
NAND_RB2	E6	Input	Ready busy	GIO_P5 CAM_SCLK	D	Leave open.
NAND_RB1	E7	Input	Ready busy	GIO_P4	D	Leave open.
NAND_CE[3:0]	T5, R5, G5, F5	Output	Chip enable	GIO_P[10:7]	D	Leave open.

(18) JTAG signals (VIO18 / VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DEBUG_EN Note	H16	Input	JTAG	–	J	Leave open.
JT0_TCK	E16	Input	JTAG	–	C	Leave open.
JT0_TRSTB	D17	Input	JTAG	–	C	Leave open.
JT0_TMS	B16	Input	JTAG	–	D	Leave open.
JT0_TDI	C16	Input	JTAG	–	D	Leave open.
JT0_TDO	D16	Output	JTAG	–	D	Leave open.
JT0_RTCK	C17	Output	JTAG	–	D	Leave open.

Note VIO18

(19) Test signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
UTEST	H17	Input	Test pin (usually fixed to 0)	–	E	“L” level hold.
TESTRSTB	E17	Input	Asynchronous reset for testing	–	N	Leave open.
TRSTB	E18	Input	Test pin	–	M	Leave open.
TE1	H12	Input	Test pin	–	Q	Leave open.
TE2	E11	Input	Test pin	–	R	Leave open.

(20) Power supply

Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
V	A7, A13, A20, B7, B13, B20, E1, E2, F23, F24, L21, L22, U1, U2, U3, U4, U5, U21, U22, Y11, AA11, AC5, AC18, AD5, AD18	–	Core power supply (1.2 V)	–	–
VIO18	A21, B21, E3, E4, L23, L24, U23, U24, AA18, AB7, AB11, AB18, AC7, AC11, AD7, AD11	–	IO power supply (1.8 V system)	–	–
VIO3	A14, B14, C7, C14, D7, D14, M1, M2, M3, M4, Y1, Y2, Y3, Y4	–	IO power supply (3 V system)	–	–
VA1	C11, D11	–	PLL power supply (1.2V)	–	–
VA2	A10, B10	–	PLL power supply (1.2V)	–	–
VA3	A12, B12	–	PLL power supply (1.2V)	–	–
VDDQ_DDR	G1, G2, P3, P4, P5, W1, W2	–	DDR power supply (1.8V)	–	–
VDD_DDR	G3, G4, H21, H22, H23, H24, N21, N22, N23, N24, P1, P2, W3, W4, W21 ,W22, W23, W24	–	DDR power supply (1.8V)	–	–

(21) GND

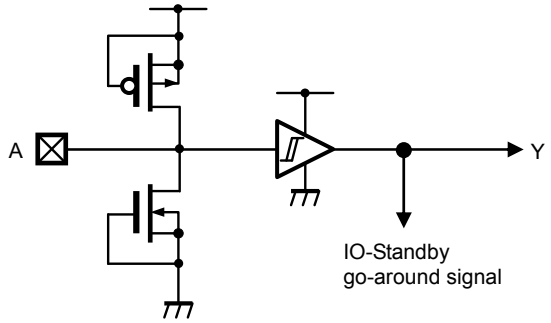
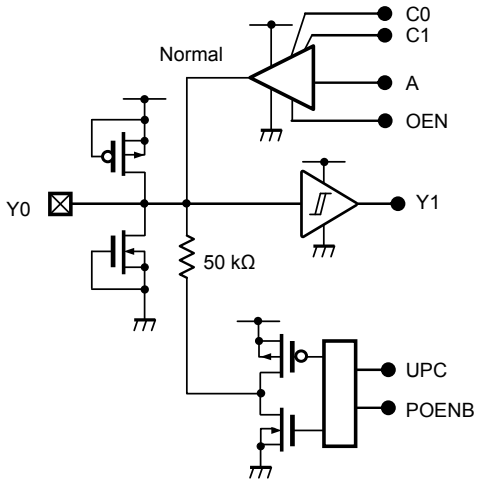
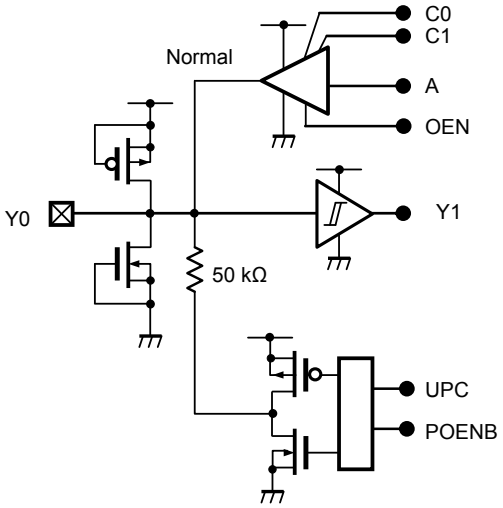
Pin Name	Pin No.	Function
G	A1, A2, A3, A6, A11, A15, A19, A22, A23, A24, B1, B2, B6, B11, B15, B19, B23, B24, C1, C6, C15, C24, D6, D15, E15, F1, F2, F3, F4, F6, G21, G22, G23, G24, H11, H15, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17,K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M21, M22, M23, M24, N1, N2, N3, N4, N5, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, T8, T9, T10, T11, T14, T15, T16, T17, U8, U9, U10, U11, U17, V1, V2, V3, V4, V5, V21, V22, V23, V24, AA6, AA10, AA15, AA19, AB1, AB6, AB10, AB15, AB19, AB24, AC1, AC2, AC6, AC10, AC15, AC19, AC23, AC24, AD1, AD2, AD3, AD6, AD10, AD15, AD19, AD22, AD23, AD24	GND

(22) Other

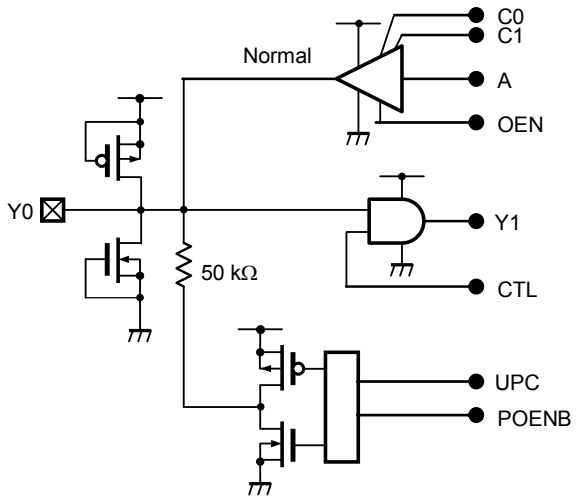
Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
IC	K17, T12, T13, U12, U13, U14, U15, U16, W5, Y5, Y6, Y7, Y8, Y9, Y10, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, AA3, AA4, AA5, AA7, AA8, AA9, AA12, AA13, AA14, AA16, AA17, AA20, AB3, AB4, AB5, AB8, AB9, AB12, AB13, AB14, AB16, AB17, AB20, AC3, AC4, AC8, AC9, AC12, AC13, AC14, AC16, AC17, AC20, AD4, AD8, AD9, AD12, AD13, AD14, AD17, AD16, AD20	–	Internally-connected pins	–	–

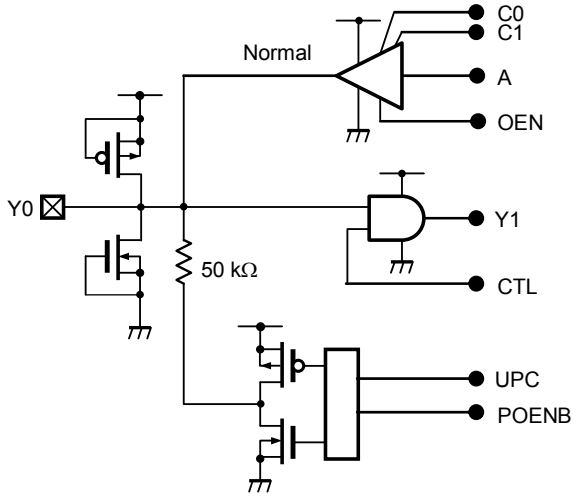
1.3 I/O Circuits

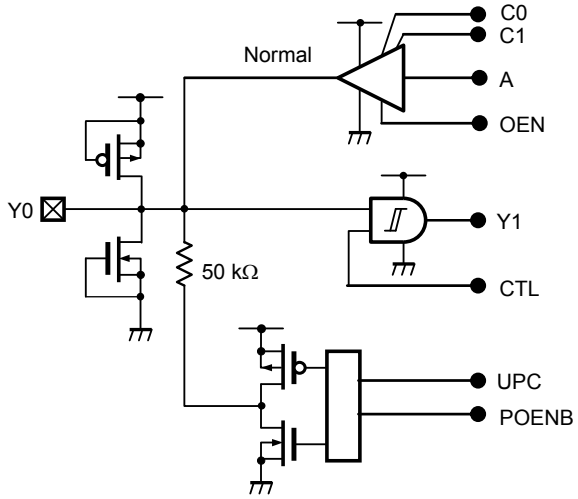
(1/4)

Type A	Description
	Input buffer Schmitt (VIO3) w / IO-Standby Control Other IO buffers are fixed on the time of Power OFF mode in POW OFF state of appendix D by inputting the Low level to this buffer. **Remark** In the Power-off mode, pins remain in a Hi-Z state (input) and the signals are passed through this buffer.
Types B, E	**Description**
	Bidirectional buffer Schmitt (type B = VIO3, type E = VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state • Resistance = 50 kΩ (typ.)
Type C	**Description**
	Bidirectional buffer Schmitt (VIO3) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state (masked by 0 internally) • Resistance = 50 kΩ (typ.)

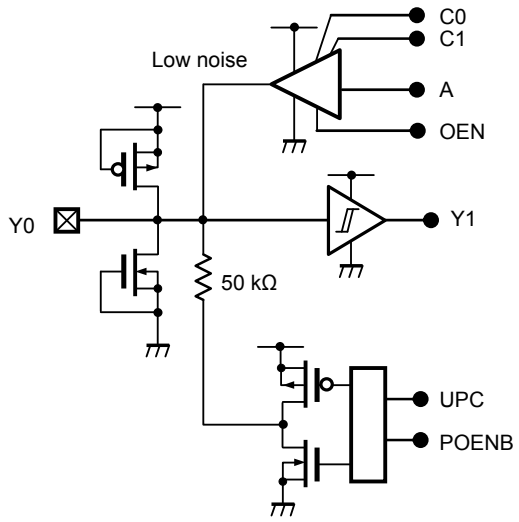
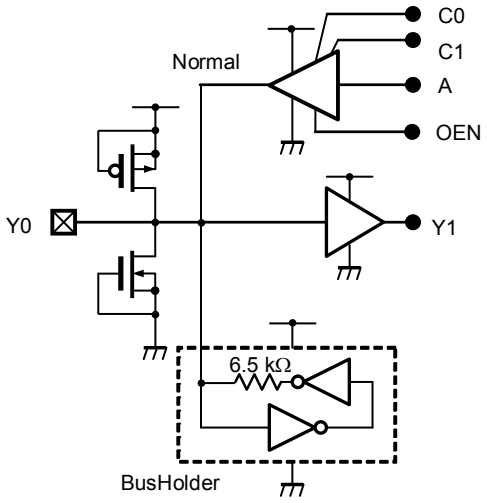
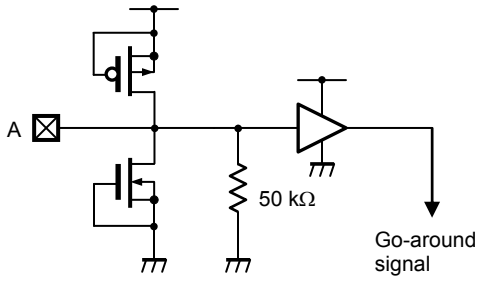
(2/4)

Type D	Description
	Bidirectional buffer AND (VIO3) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state (masked by 0 internally) • Resistance = 50 kΩ (typ.)

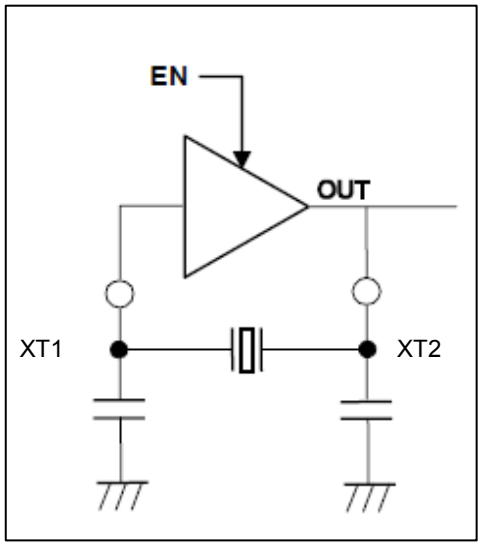
Types G	Description
	Bidirectional buffer AND (VIO18) w / IOLH control Normal / Pull-up 50 kΩ Pull-down 50 kΩ • During power-off: Type G: Pins are pulled down (masked by 0 internally) • Resistance = 50 kΩ (typ.)

Type J	Description
	Bidirectional buffer AND, Schmitt (VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins are pulled down (masked by 0 internally) • Resistance = 50 kΩ (typ.)

(3/4)

Types M, N	Description
	Bidirectional buffer Schmitt / LowNoise (VIO18) w / IOLH control Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Type M: Pins are pulled down (masked by 0 internally) Type N: Pins are pulled up (masked by 0 internally) • Resistance = 50 kΩ (typ.)
Type P	**Description**
	Bidirectional buffer (VIO18) w / IOLH control bus holder • During power-off: Pins output a low level (masked by 0 internally) • Resistance = 6.5 kΩ (typ.)
Types Q, R	**Description**
	Test buffer (VIO18) Types Q and R are buffers used exclusively for testing. Leave open when used in the actual device. (Always pull down the pins (typ. 50 kΩ)

(4/4)

Type Z	Description
	oscillator

2. ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V	1.2 V system	−0.5 to +1.8	V
	V_{IO18}	1.8 V system (I/O)	−0.5 to +2.5	V
	V_{IO3}	3 V system (I/O)	−0.5 to +4.6	V
	V_{DD_DDR} V_{DDQ_DDR}	Power supply for memories	−0.5 to +2.3	V
Input voltage	V_{I_18}	1.8 V system (I/O)	−0.5 to V_{IO18} + 0.5	V
	V_{I_33}	3 V system (I/O)	−0.5 to V_{IO3} + 0.5	V
Output voltage	V_{O_18}	1.8 V system (I/O)	−0.5 to V_{IO18} + 0.5	V
	V_{O_33}	3 V system (I/O)	−0.5 to V_{IO3} + 0.5	V
Storage temperature	T_{stg}	−	−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Note Instantaneous input of a voltage in the range of −0.8 to V_{DD12} + 0.8 V is allowed as long as capacitive coupling is implemented.

2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V	1.2 V system, during normal operation	1.1	1.2	1.3	V
		Memory retention voltage[Note 1]	0.64	−	−	V
	$V_{\_PLL}$	1.2 V system (PLL power supply, pin: VA)	1.1	1.2	1.3	V
	V_{IO18}	1.8 V system (I/O power supply)	1.7	1.8	1.9	V
	V_{IO3}	3 V system (I/O power supply)	2.7	−	3.6	V
	V_{DD_DDR} V_{DDQ_DDR}	Power supply for memories	1.7	1.8	1.9	V
Oscillation start voltage[Note 2]	V_{OSC_S}	−	1.7	−	−	V
Oscillation start voltage[Note 3]	V_{OSC_H}	−	1.7	−	−	V
Operating ambient temperature	T_A	−	−20	−	+70	°C

Notes 1. This is the voltage that guarantees retention of data in the internal SRAM when the voltage drops during normal operation.

2. This is the voltage at which oscillation always starts after power-on.

3. This is the voltage that guarantees oscillation when the voltage drops during normal operation.

2.3 Capacitance

(T_A = +25°C, f = 1 MHz, unmeasured pins returned to 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	1.8 V	3	–	5	pF
		2.8 V	2	–	4	pF
Output capacitance	C_O	1.8 V	3	–	5	pF
		2.8 V	2	–	4	pF
I/O capacitance	C_{IO}	1.8 V	3	–	5	pF
		2.8 V	2	–	4	pF

2.4 DC Characteristics

2.4.1 VIO18

(Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load[Note 1]	$V_{IO18} - 0.1$	−	−	V
Output voltage, low	V_{OL}	No DC load[Note 1]	−	−	0.1	V
Input voltage, high	V_{IH}	I/O pins and monitor pins	$0.65 \times V_{IO18}$	−	$V_{IO18} + 0.5$	V
Input voltage, low	V_{IL}	I/O pins and monitor pins	−0.5	−	$0.35 \times V_{IO18}$	V
Output current, high $V_{OH} = V_{IO18} - 0.4$ V[Note 2]	I_{OUT_H1}	2 mA setting[Note 3]	1.7	−	−	mA
	I_{OUT_H2}	4 mA setting[Note 3]	3.7	−	−	mA
	I_{OUT_H3}	6 mA setting[Note 3]	5.7	−	−	mA
	I_{OUT_H4}	8 mA setting[Note 3]	7.7	−	−	mA
	I_{OUT_H5}	12 mA setting[Note 3]	11.0	−	−	mA
Output current, low $V_{OL} = 0.4$ V[Note 2]	I_{OUT_L1}	2 mA setting[Note 3]	1.7	−	−	mA
	I_{OUT_L2}	4 mA setting[Note 3]	3.7	−	−	mA
	I_{OUT_L3}	6 mA setting[Note 3]	5.7	−	−	mA
	I_{OUT_L4}	8 mA setting[Note 3]	7.7	−	−	mA
	I_{OUT_L5}	12 mA setting[Note 3]	11.0	−	−	mA
Hysteresis voltage	V_H	Schmitt input	$0.20 \times V_{IO18}$	−	$0.63 \times V_{IO18}$	V
Negative trigger voltage	V_N	Schmitt input	$0.53 \times V_{IO18} - 0.66$	−	$0.35 \times V_{IO18}$	V
Positive trigger voltage	V_P	Schmitt input	$0.68 \times V_{IO18}$	−	$0.83 \times V_{IO18}$	V
Input leakage current, high	I_{L_H}	$V_I = V_{IO18}$	−	−	1	μA
Input leakage current, low	I_{L_L}	V_I = GND	−	−	1	μA
Pull-up resistance	R_{PU}	−	40	−	65	kΩ
Pull-down resistance	R_{PD}	−	40	−	65	kΩ
Bus-holder hold resistance	R_{BH}	Bus-holder series resistance	5	−	11	kΩ
Pull-up pin current	I_{PU}	−	−	−	50	μA
Pull-down pin current	I_{PD}	−	−	−	50	μA

Notes 1. The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the I/O buffer output current drive switch register.

2.4.2 VIO3

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load[Note 1]	$V_{IO3} - 0.1$	–	–	V
Output voltage, low	V_{OL}	No DC load[Note 1]	–	–	0.1	V
Input voltage, high	V_{IH}	I/O pins and monitor pins	2.0	–	$V_{IO3} + 0.5$	V
Input voltage, low	V_{IL}	I/O pins and monitor pins	–0.5	–	0.8	V
Output current, high $V_{OH} = V_{IO3} - 0.4$ V[Note 2]	I_{OUT_H1}	2 mA setting[Note 3]	1.7	–	–	mA
	I_{OUT_H2}	4 mA setting[Note 3]	3.7	–	–	mA
	I_{OUT_H3}	6 mA setting[Note 3]	5.7	–	–	mA
	I_{OUT_H4}	8 mA setting[Note 3]	7.7	–	–	mA
Output current, low $V_{OL} = 0.4$ V[Note 2]	I_{OUT_L1}	2 mA setting[Note 3]	1.7	–	–	mA
	I_{OUT_L2}	4 mA setting[Note 3]	3.7	–	–	mA
	I_{OUT_L3}	6 mA setting[Note 3]	5.7	–	–	mA
	I_{OUT_L4}	8 mA setting[Note 3]	7.7	–	–	mA
Hysteresis voltage	V_H	Schmitt input	$0.11 \times V_{IO3}$	–	$0.41 \times V_{IO3}$	V
Negative trigger voltage	V_N	Schmitt input	$0.17 \times V_{IO3}$	–	$0.38 \times V_{IO3}$	V
Positive trigger voltage	V_P	Schmitt input	$0.54 \times V_{IO3}$	–	$0.65 \times V_{IO3}$	V
Input leakage current, high	I_{L_H}	$V_I = V_{IO3}$	–	–	1	μA
Input leakage current, low	I_{L_L}	V_I = GND	–	–	1	μA
Pull-up resistance	R_{PU}	50 kΩ resistor	40	–	65	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor	40	–	65	kΩ
Pull-up pin current	I_{PU}	50 kΩ resistor	–	–	90	μA
Pull-down pin current	I_{PD}	50 kΩ resistor	–	–	90	μA

Notes 1. The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. $V_{OL} = 0.4$ V, $V_{OH} = V_{IO3} - 0.4$ V. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register.

2.4.3 Standby state current (Logic)

($T_A = 25°C$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current	I_{DD_L0}	Logic power supply L0 + L2 on, f = 0 Hz, V = 0.75 V	–	130	400	μA
		Logic power supply L0 on, f = 0 Hz, V = 0.75 V	–	100	300	μA
		Logic power supply L0 on, f = 0 Hz, V = 1.2 V	–	340	–	μA
	I_{DD_IO18}	IO power supply f = 0 Hz, $V_{IO18} = 1.8$ V	–	–	10	μA
	I_{DD_IO3}	IO power supply f = 0 Hz, $V_{IO3} = 2.85$ V	–	–	10	μA

2.4.4 Standby state current (Mobile DDR SDRAM)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current (Deep power-down mode)	DDR IDD7	CKE≦0.2V	−	−	10	μA

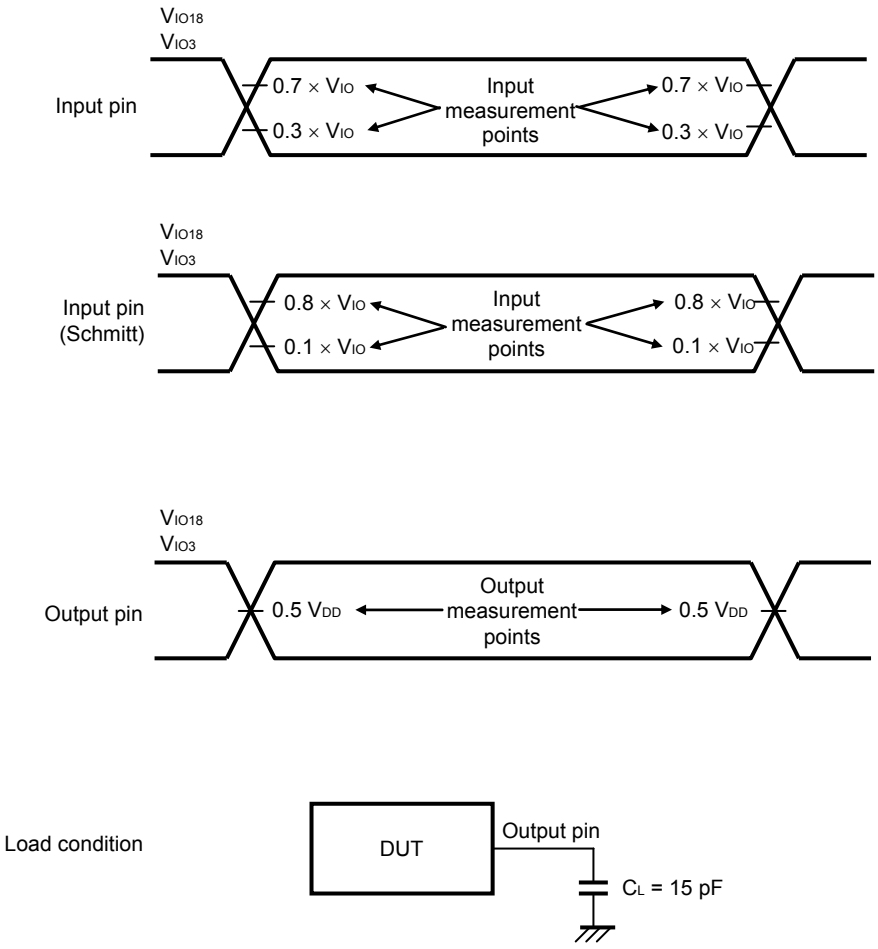
2.4.5 Self refresh current

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PASR = “000” (Full)	DDR IDD6	-25°C ≦DDR_T_J≦+85°C CKE≦0.2V	−	−	500	μA
PASR = “001” (2BK)			−	−	400	μA
PASR = “010” (1BK)			−	−	300	μA

2.5 AC Characteristics

2.5.1 AC test I/O measurement points

Figure 2-1. AC Test I/O Measurement Points



Remark Excluding the OSC pin. Unless specified otherwise, the load of C_L is assumed to be 15 pF.
Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition

2.5.2 System control

(1) Clock (input timing requirements)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
C32K frequency	$f_{clkC32K}$	–	–	32.768	–	kHz
C32K rise/fall time	t_{rfC32K}	10 to 90%	–	–	1	μs
32 kHz input clock duty ratio	$I_{dutyC32K}$	–	40	50	60	%
32 kHz input clock jitter	$I_{jitterC32K}$	–	–20	–	20	ns
OSC oscillation frequency range	$f_{C(OSC)}$	Internal oscillator (OSC12M_CKI or OSC12M_CKO) (with crystal resonator DSX530GA; made by Daishinku)	–	–	13	MHz
OSC clock stabilization time	t_{STAB12}	CI = CO = 15 pF The oscillating frequency : 12MHz (with crystal resonator DSX530GA; made by Daishinku)	–	0.5	1	ms

Figure 2-2. Clock Timing

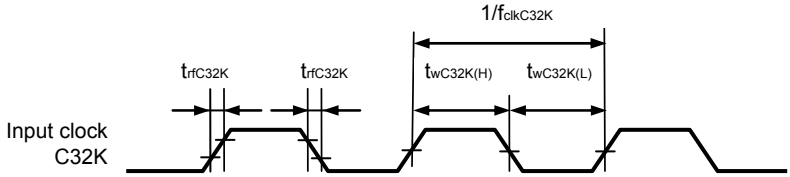
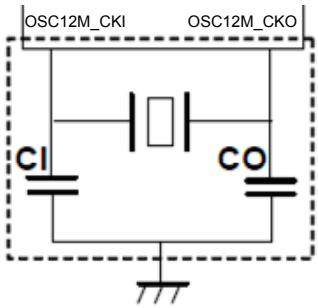


Figure 2-3. Recommended Oscillator



Cautions 1. Keep the wiring length between the oscillator and the OSC12M_CKI and OSC12M_CKO pins as short as possible.

2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.

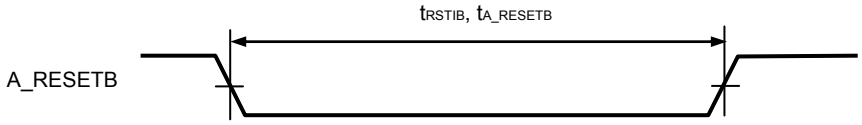
3. Thoroughly evaluate matching of the resonator.

(2) Reset (A_RESETB)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A_RESETB low-level width	t_{A_RESETB}	–	6	–	–	ms

Remark In the case of a hardware reset.

Figure 2-4. Reset Timing



(3) Power supply start-up Timing (without power supply -> Normal)

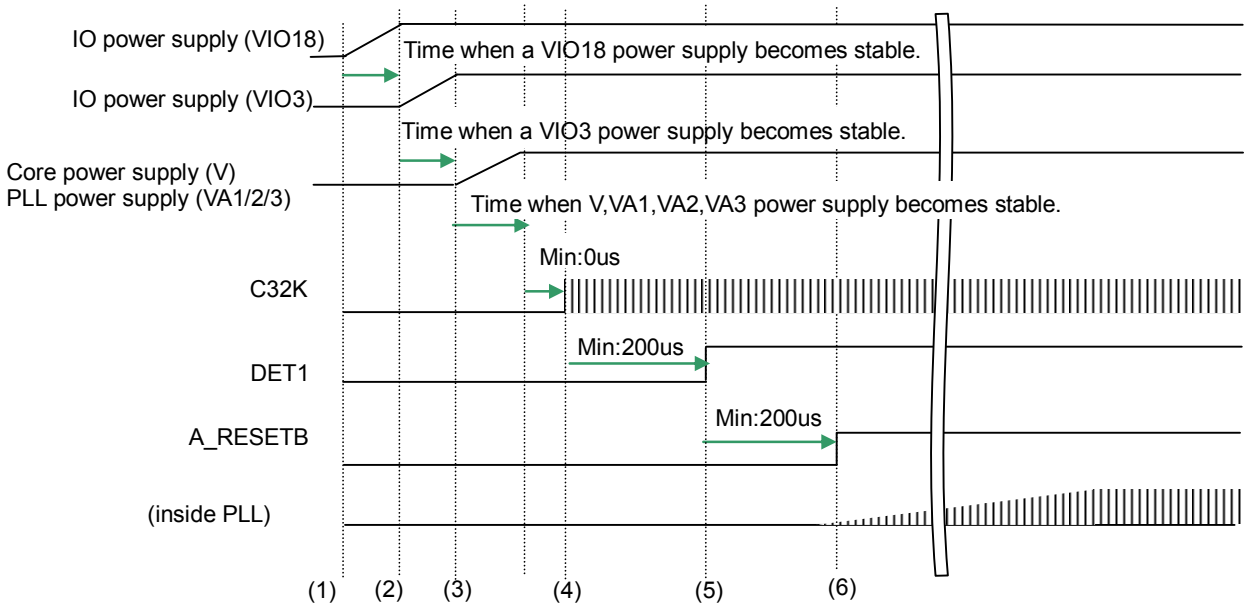


Figure 2-5. Power supply start-up timing

Remarks "Stable" means that each power supply becomes the specification minimum voltage.

The timing figure which starts from the "Without power supply".

(1) IO power supply (VIO18) is supplied, and stands by until a power supply becomes stable.
(2) IO power supply (VIO3) is supplied, and stands by until a power supply becomes stable.
(3) Corepower supply (V) and PLL power supply (VA1/2/3) are supplied, and stands by until a power supply becomes stable.
(4) RTC clock 32.768kHz (C32K) is input.
(5) DET1 is signal is started.
(6) A_RESETB signal rising (reset release), and PLL begins to oscillate.

(4) Power supply start-up Timing (DeepSleep<- -> Normal)

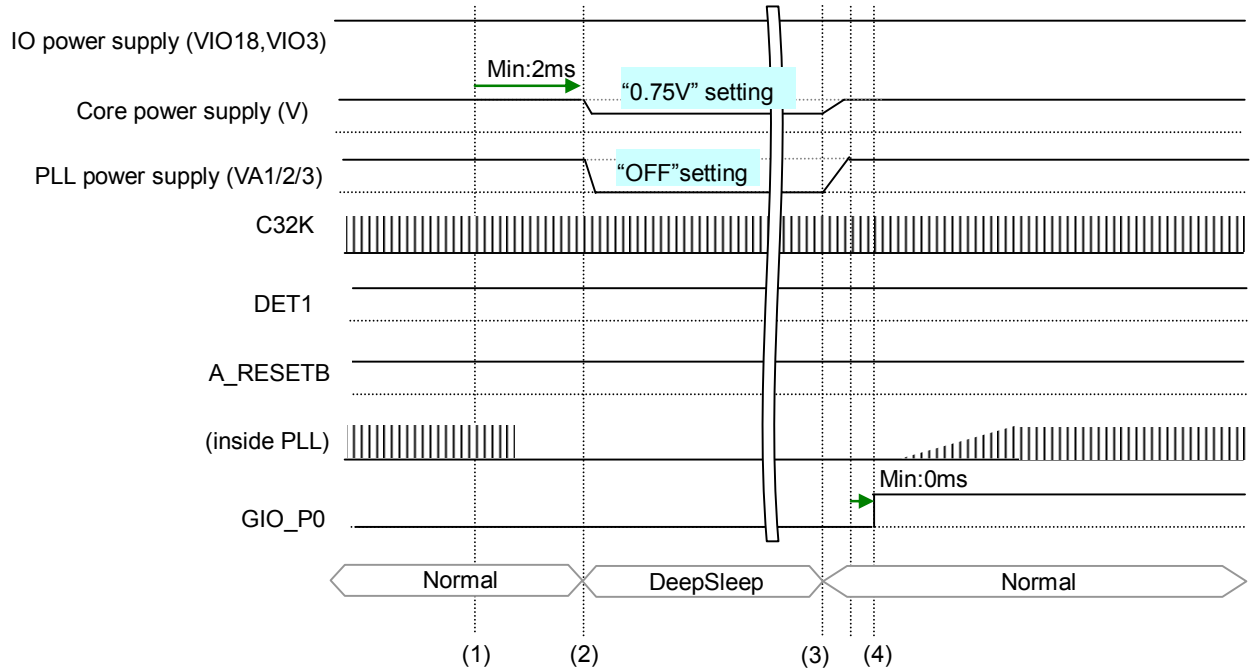


Figure 2-6. DeepSleep Normal timing

(1) EM1-D512 sends the command to Power Management IC by SPI Interface. The contents of the command are as follows. Core power supply (V) voltage is changed to 0.75 from 1.2V. PLL power supply (VA1/2/3) is stopped.

(2) Power Management IC changes the Core power supply (V) to 0.75V from 1.2V in at least 2 ms later and stops PLL power supply (VA1/2/3). EM1-D512 does the preparations to transfer to the DeepSleep state between (1) and (2).

(3) Core power supply (V) voltage is changed to 1.2V from 0.75V. VPLL power supply (VA1/2/3) is supplied.

(4) GIO_P0 signal rising and inside PLL begins to oscillate. EM1-D512 is transit of state from DeepSleep to Normal after inside PLL stable.

(5) Power supply start-up Timing (PowerOff<- -> Normal)

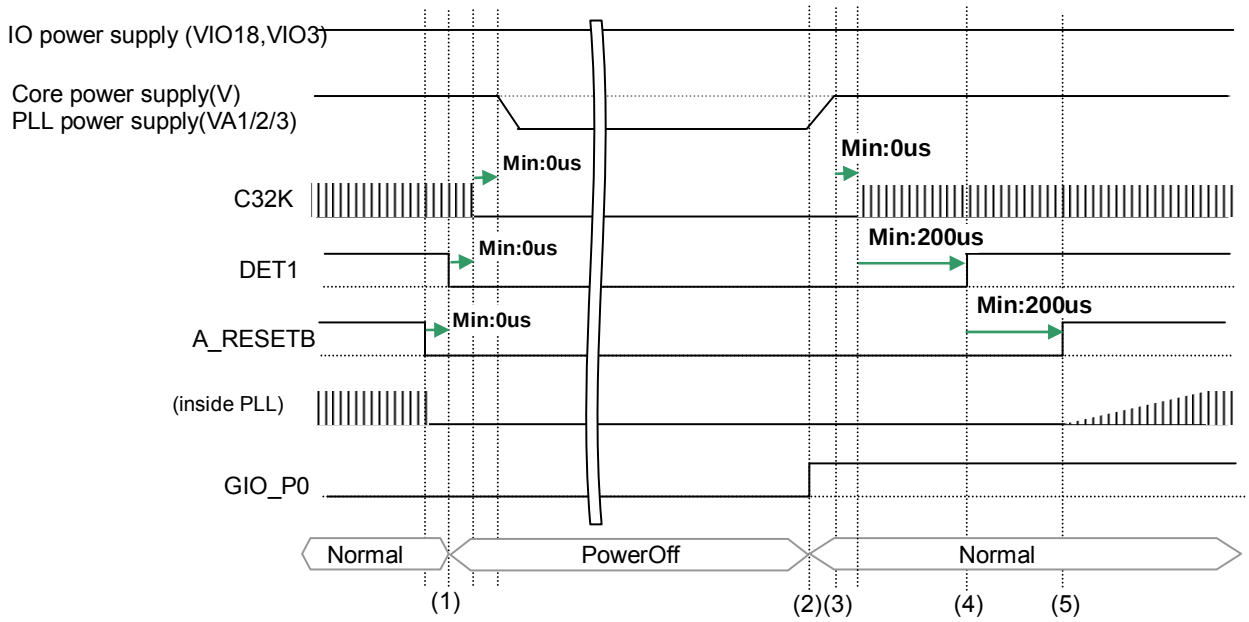


Figure 2-7. PowerOff Normal timing

(1) A_RESETB signal and DET1 signal are falling, and RTC clock (C32K) is stop. Next Core power supply and PLL power supply are stopped at the same time.

(2) Core power supply (V) and PLL power supply (VA1/2/3) are supplied same time, and stand by until a power supplies become stable.

(3) RTC clock 32.768kHz (C32K) is input.
GIO_P0 signal rising. It's to make EM1-D512 recognizes that it's different from "Without power supply".

(4) DET1 is signal is started.

(5) A_RESETB signal rising (reset release), and inside PLL begins to oscillate.

2.5.3 Asynchronous bus (AB0) interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Asynchronous single read access time	t_{201}	**Note**	(1 + T0 + T1 + T2) × Tf – 3	–	(2 + T0 + T1 + T2) × Tf + 3	ns
CSZ rise to ADVZ fall	t_{202}	**Note**	Tf – 3	–	2Tf + 3	ns
ADVZ active width	t_{203}	AB0_ADVZ = Low	Tf – 3	–	Tf + 3	ns
Lower ADD for ADMUX hold time	t_{204}	–	T0 × Tf – 3	–	T0 × Tf + 3	ns
Delay time from ADVZ rise to read signal output	t_{205}	Falling edge of AB0_RDZ	T0 × Tf – 3	–	T0 × Tf + 3	ns
Read signal active width	t_{206}	AB0_RDZ = Low	T1 × Tf – 3	–	T1 × Tf + 3	ns
Delay time from RDZ rise to CSZ fall output	t_{207}	Rising edge of AB0_RDZ	T2 × Tf – 3	–	T2 × Tf + 3	ns
CS assert interval time	t_{208}	–	CSInt × Tf – 3	–	–	ns
Asynchronous _RDATA setup time	t_{209}	Rising edge of AB0_RDZ	15	–	–	ns
Asynchronous _RDATA hold time	t_{210}	Rising edge of AB0_RDZ	0	–	–	ns
Delay time from address determination to RDZ fall	t_{211}	Falling edge of AB0_RDZ**Note**	(1 + T0) × Tf – 8	–	–	ns
Delay time from CSZ fall to RDZ rise output	t_{212}	Falling edge of AB0_RDZ**Note**	(1 + T0) × Tf – 3	–	–	ns
Asynchronous single write access time	t_{220}	**Note**	(1 + T0 + $T1_W$ + $T2_W$) × Tf – 3	–	(2 + T0 + $T1_W$ + $T2_W$) × Tf + 3	ns
Delay time from ADVZ rise to write signal output	t_{221}	Rising edge of AB0_WRZ	T0×Tf – 3	–	T0× Tf + 3	ns
Write signal active width	t_{222}	AB0_WRZ = Low	$T1_W$ × Tf – 3	–	$T1_W$ × Tf + 3	ns
Delay time from WRZ rise to CSZ fall output	t_{223}	Rising edge of AB0_WRZ	$T2_W$ × Tf – 3	–	$T2_W$ × Tf + 3	ns
Asynchronous _WDATA output hold time	t_{224}	Rising edge of AB0_WRZ	$T2_W$ × Tf – 8	–	–	ns
Delay time from address determination to WRZ fall	t_{225}	Falling edge of AB0_WRZ**Note**	(1 + T0) × Tf – 8	–	–	ns
Delay time from CSZ fall to WRZ fall output	t_{226}	Falling edge of AB0_WRZ**Note**	(1 + T0) × Tf – 3	–	–	ns

Note The time from the CSB falling edge to the ADV falling edge (Tf) can be shortened by setting a register.

Remark Tf = 1/4 of AB0_CLK. (When frequency ratio 1/4 is usually the time of the state (AB0_CLK:FLASH_CLK = 2:1).
T0, T1, T2, CSInt: Values set to read the wait timing control register (AB0_CSxWAITCTRL)
$T1_W$, $T2_W$: Values set to write the wait timing control register (AB0_CSxWAITCTRL_W)

Figure 2-8. Asynchronous Single Read Timing

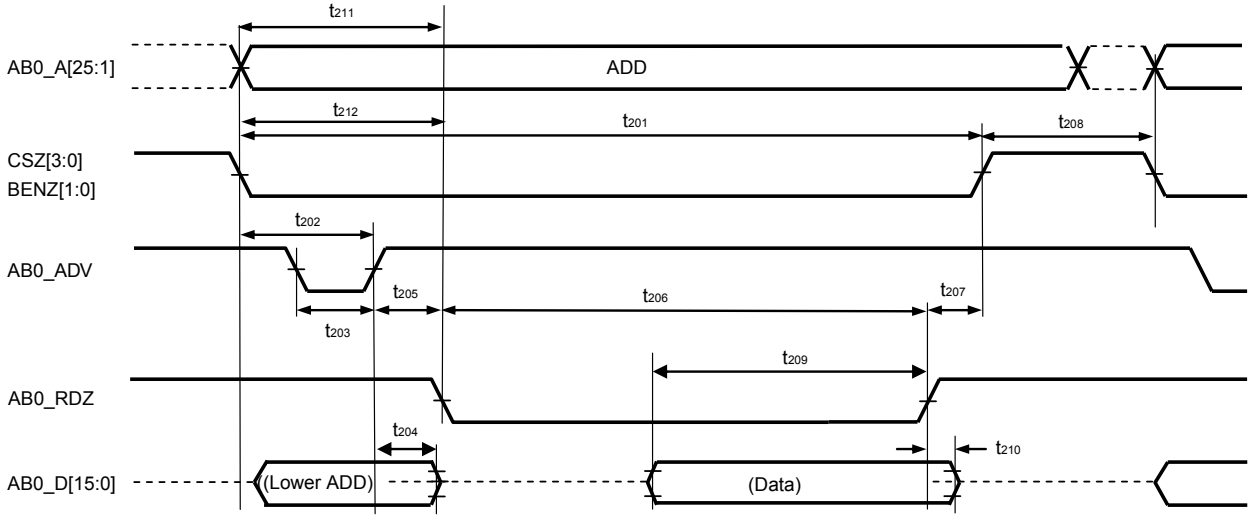
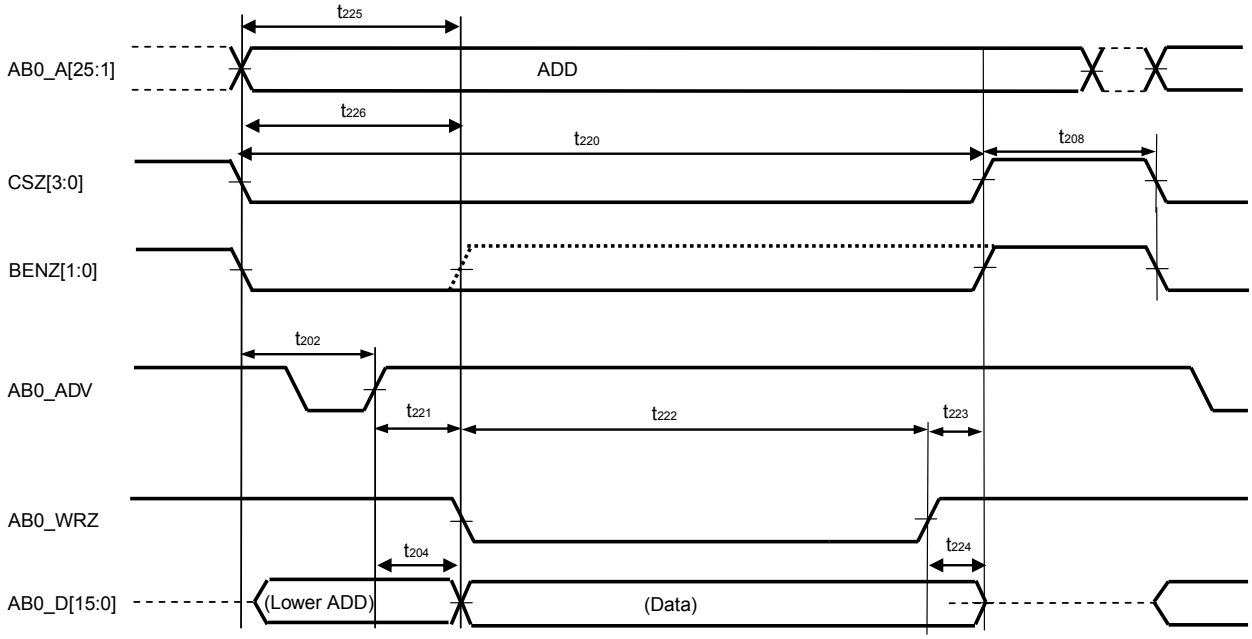


Figure 2-9. Asynchronous Single Write Timing



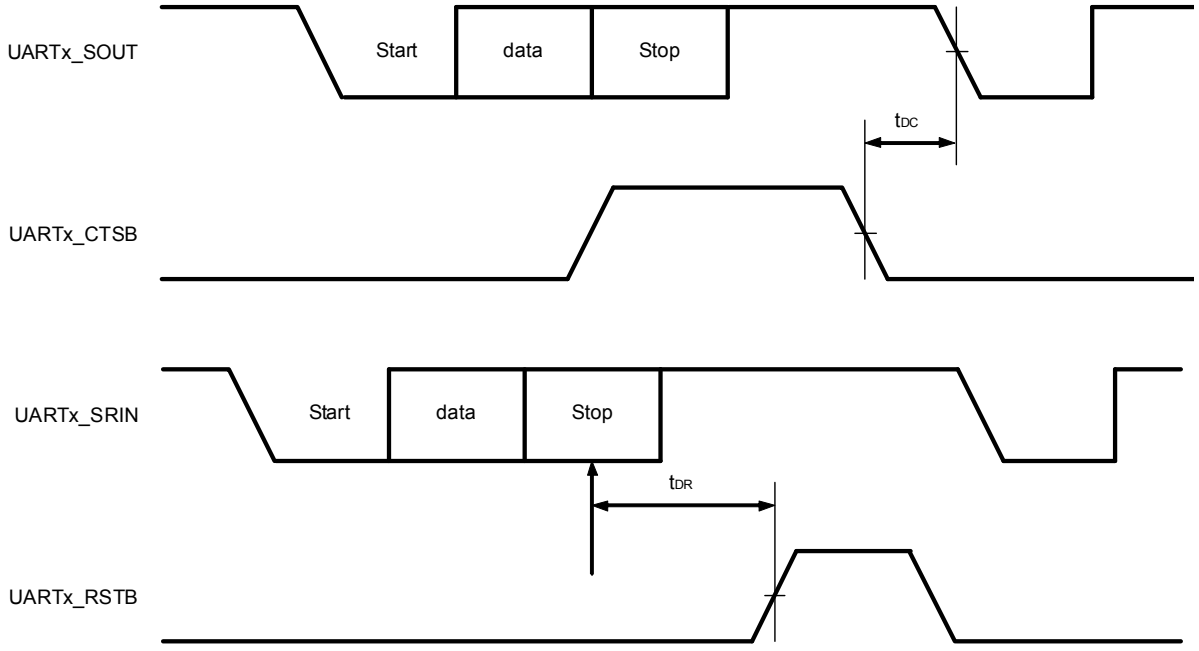
2.5.4 UART interface

(IO buffer drive capability: 2 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UARTx_SOUT output delay time	t_{DC}	Falling edge of UARTx_CTSB	–	–	4	RCLK
UARTx_RTSB output delay time	t_{DR}	Center of UARTx_SRIN stop bit	–	–	3	RCLK

Remark RCLK: 1/16 of baud rate clock cycle

Figure 2-10. UART Interface Timing



Remark x = 0 to 2 (UARTx_CTSB and UARTx_RSTB for UART0 and UART2 are pins and are not provided for UART1.)

2.5.5 IIC interface

(IO buffer drive capability: 2 mA)

Parameter	Symbol	Conditions	Standard Mode[Note 1]		High-Speed Mode[Note 1]		Unit
			MIN.	MAX.	MIN.	MAX.	
IIC_SCL clock frequency	f_C	–	0	70	0	341	kHz
IIC bus free time	t_{BF}	Interval between stop and start conditions	4.7	–	1.3	–	μs
IIC hold time[Note 2]	t_{H1}	–	4.0	–	0.6	–	μs
IIC hold time (SCL clock)	t_{WL}	"Low" state	4.7	–	1.3	–	μs
	t_{WH}	"Hi" state	4.0	–	0.6	–	μs
IIC setup time	t_{SU1}	Start condition Restart condition	4.7	–	0.6	–	μs
IIC data setup time	t_{SU2}	–	250	–	100[Note 3]	–	ns
IIC rise time	t_R	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC fall time	t_F	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC setup time	t_{SU3}	Stop condition	4.0	–	0.6	–	μs
IIC data hold time	t_{H2}	Clock fall output	5.0	–	–	–	μs
		Clock fall input	0	3.45	0[Note 5]	0.9[Note 6]	μs
Capacitance load of each IIC bus line	C_b	–	–	400	–	400	pF

Notes 1. Select the standard mode or high-speed mode by using the SMC0 bit of the IIC0 clock select register (IICCL0).

2. At the start condition, the first clock pulse is generated after the hold time.

3. The high-speed mode I^2C bus can be used in the standard-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

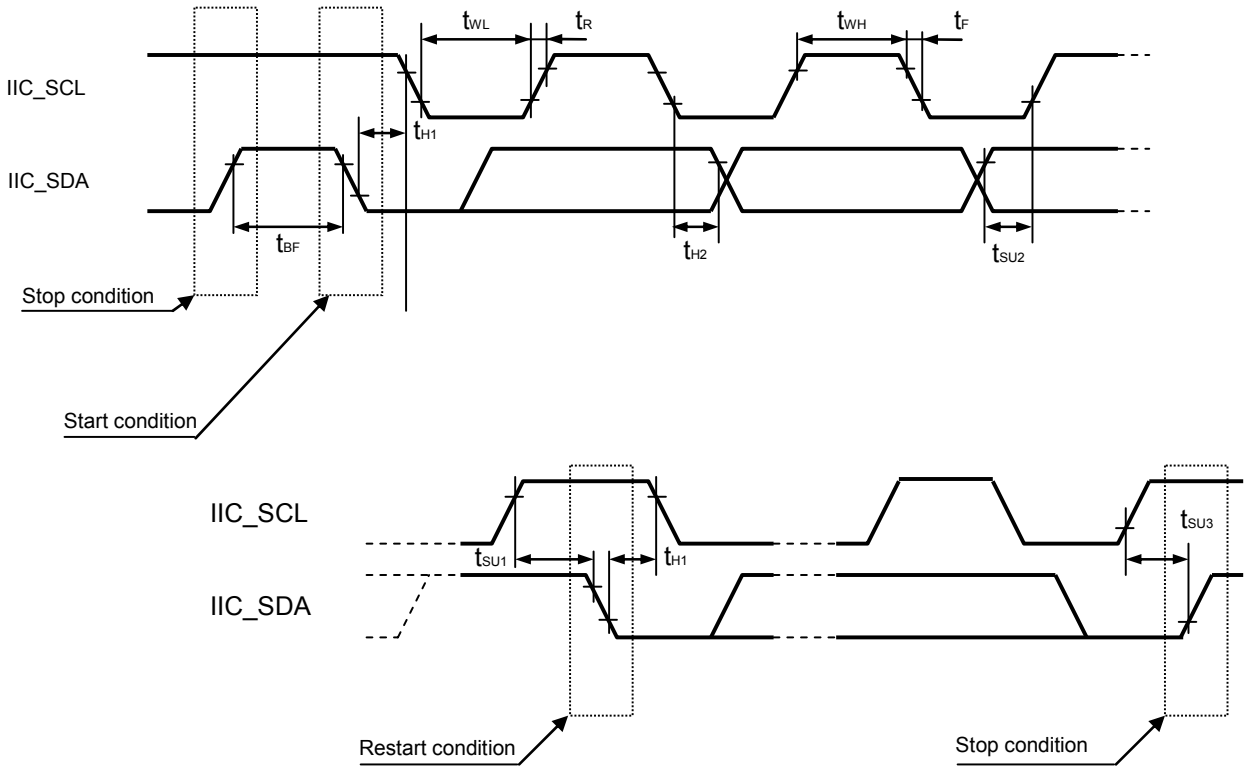
- If the system does not extend the IIC_SCL signal's low state hold time: $t_{SU2} \geq 250$ ns

4. Do not input noise exceeding the hysteresis width of the 1.8 V system IO Schmitt buffer during a rise or fall time.

5. The system requires a minimum of 300 ns hold time internally for the SDA signal (at V_{IH} (MIN.) [0.7 V_{DD2}] of IIC_SCL signal) in order to occupy the undefined area at the falling edge of IIC_SCL.

6. If the system does not extend the IIC_SCL signal low hold time (t_{WL}), only the maximum data hold time (t_{H2}) needs to be satisfied.

Figure 2-11. IIC Bus Interface Timing



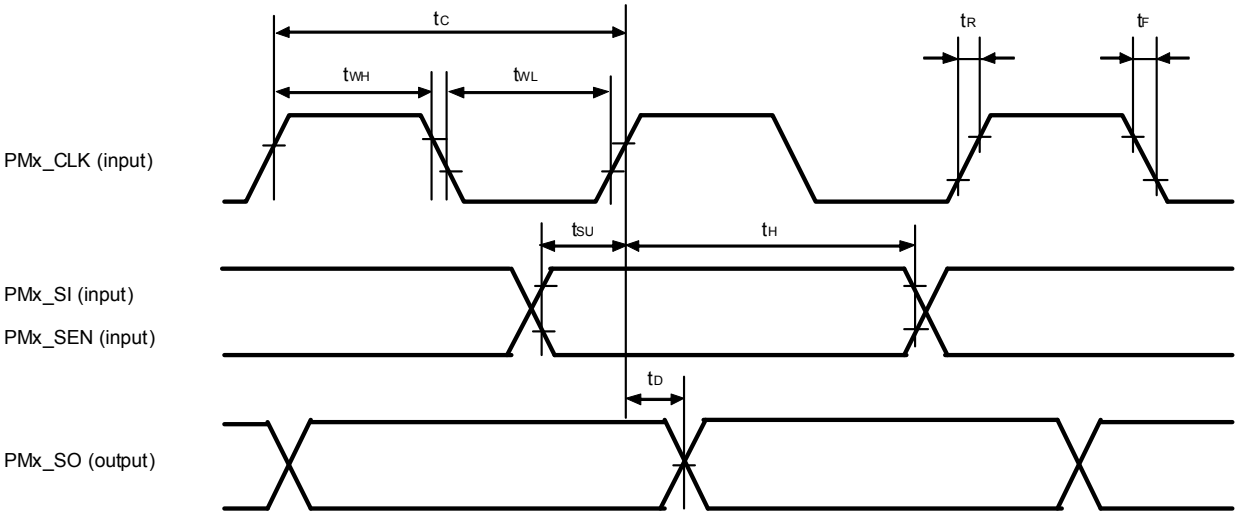
2.5.6 Audio/Voice interface

(1) Slave mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PMx_CLK cycle time	t_C	–	100	–	–	ns
PMx_CLK high-level width	t_{WH}	–	40	–	–	ns
PMx_CLK low-level width	t_{WL}	–	40	–	–	ns
Clock rise time	t_R	–	–	–	10	ns
Clock fall time	t_F	–	–	–	10	ns
PMx_SI, PMx_SEN setup time	t_{SU}	Rising and falling edges of PMx_CLK	20	–	–	ns
PMx_SI, PMx_SEN hold time	t_H	Rising and falling edges of PMx_CLK	20	–	–	ns
PMx_SO output delay time	t_D	Rising and falling edges of PMx_CLK	0	–	20	ns

Remark Time from the valid edge
x = 0, 1

Figure 2-12. Audio/Voice Interface Timing (Slave Mode)

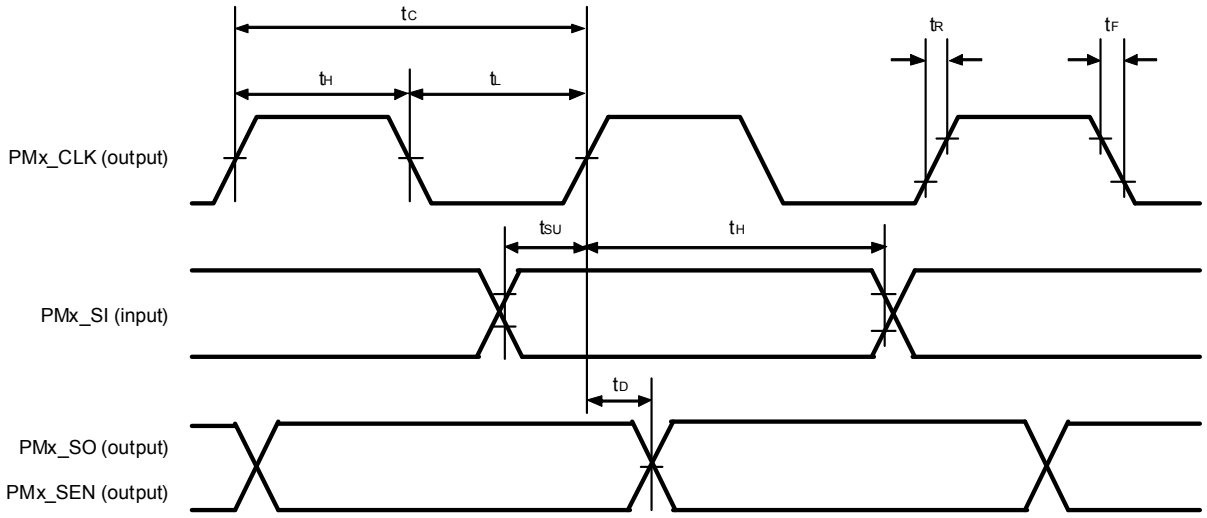


(2) Master mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PM0_CLK cycle time	t_C	–	100	–	–	ns
PM0_CLK high-level width	t_{WH}	–	40	–	–	ns
PM0_CLK low-level width	t_{WL}	–	40	–	–	ns
Clock rise time	t_R	–	–	–	10	ns
Clock fall time	t_F	–	–	–	10	ns
PMx_SI setup time	t_{SU}	–	20	–	–	ns
PM0_SI hold time	t_H	–	20	–	–	ns
PM0_SO, PM0_SEN output delay time	t_D	–	–5	–	20	ns

Remark Time from the valid edge
x = 0, 1

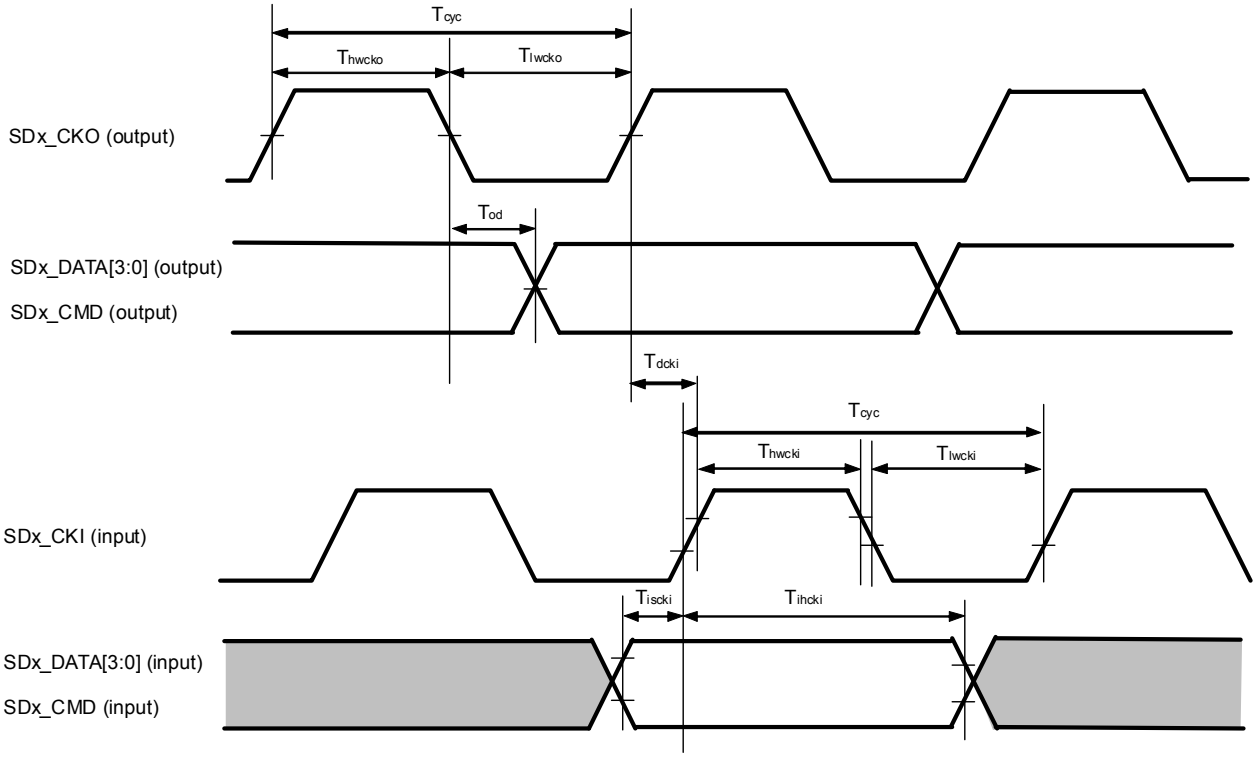
Figure 2-13. Audio/Voice Interface Timing (Master Mode)



2.5.7 SDIO interface

Parameter	Symbol	Conditions	SD0 (SDIA), SD1 (SDIB), SD2 (SDIC)			
			MIN.	TYP.	MAX.	Unit
Clock cycle	T_{cyc}	–	24.0	–	–	ns
Output clock high-level width	T_{hwcko}	–	11.5	–	–	ns
Output clock low-level width	T_{lwcko}	–	11.5	–	–	ns
Output delay	T_{od}	–	–	–	2	ns
Input clock high-level width	T_{hwcki}	–	7.5	–	–	ns
Input clock low-level width	T_{lwcki}	–	7.5	–	–	ns
Input clock delay time	T_{dcki}	–	–	–	6	ns
Setup time	T_{iscki}	–	3.5	–	–	ns
Hold time	T_{ihcki}	–	0	–	–	ns

Figure 2-14. SDIO Interface Timing

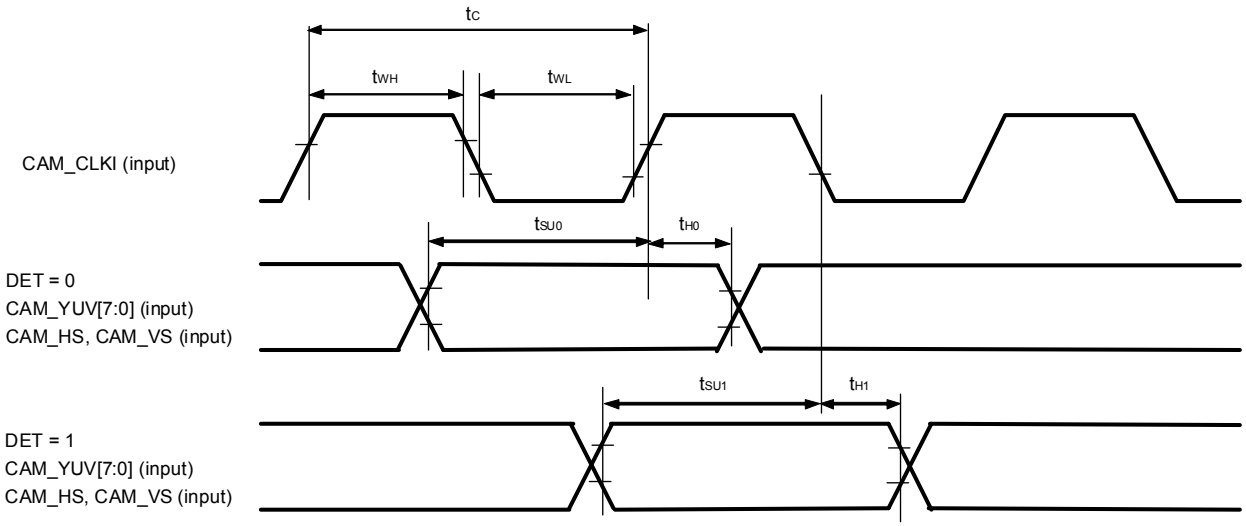


Remark x = 0 to 2

2.5.8 Camera interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CAM_CLKI input cycle	t_C	–	12.5	–	–	ns
CAM_CLKI high-level width	t_{WH}	–	4	–	–	ns
CAM_CLKI low-level width	t_{WL}	–	4	–	–	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU0}	DET = 0	5	–	–	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H0}	DET = 0	0	–	–	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU1}	DET = 1	5	–	–	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H1}	DET = 1	1	–	–	ns

Figure 2-15. Camera Interface Timing

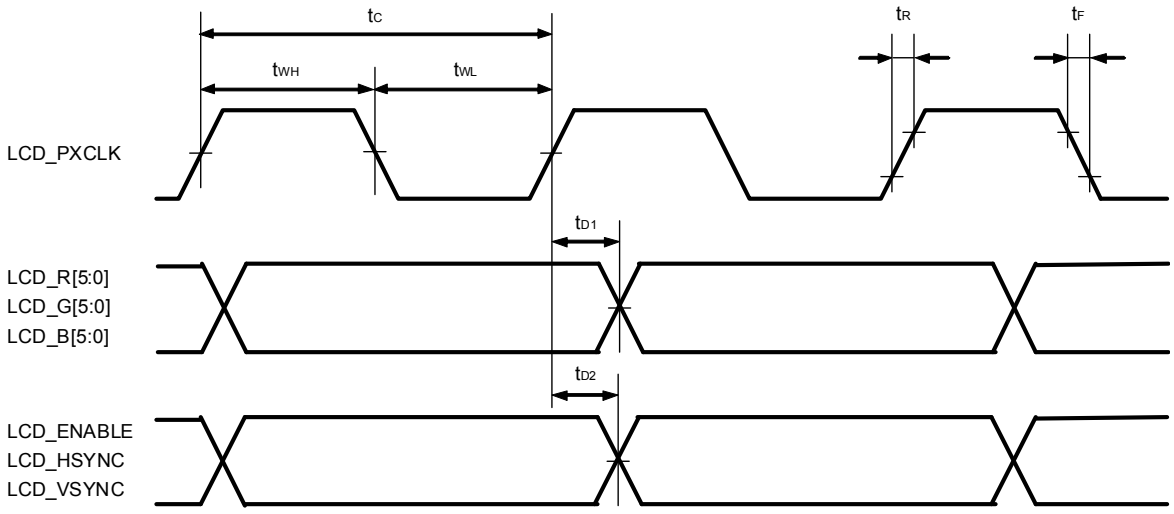


2.5.9 LCD interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD_PXCLK cycle	t_C	–	30	–	–	ns
LCD_PXCLK high-level width	t_{WH}	–	12	–	–	ns
LCD_PXCLK low-level width	t_{WL}	–	12	–	–	ns
LCD_PXCLK rise time	t_R	20 to 80%	–	–	5	ns
LCD_PXCLK fall time	t_F	80 to 20%	–	–	5	ns
Data delay time	t_{D1}	LCD_R[5:0], LCD_G[5:0], LCD_B[5:0]	0	–	10	ns
	t_{D2}	LCD_VSYNC, CD_HSYNC, LCD_ENABLE	0	–	10	ns

Remark The setting of the rise and fall timing for LCD_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

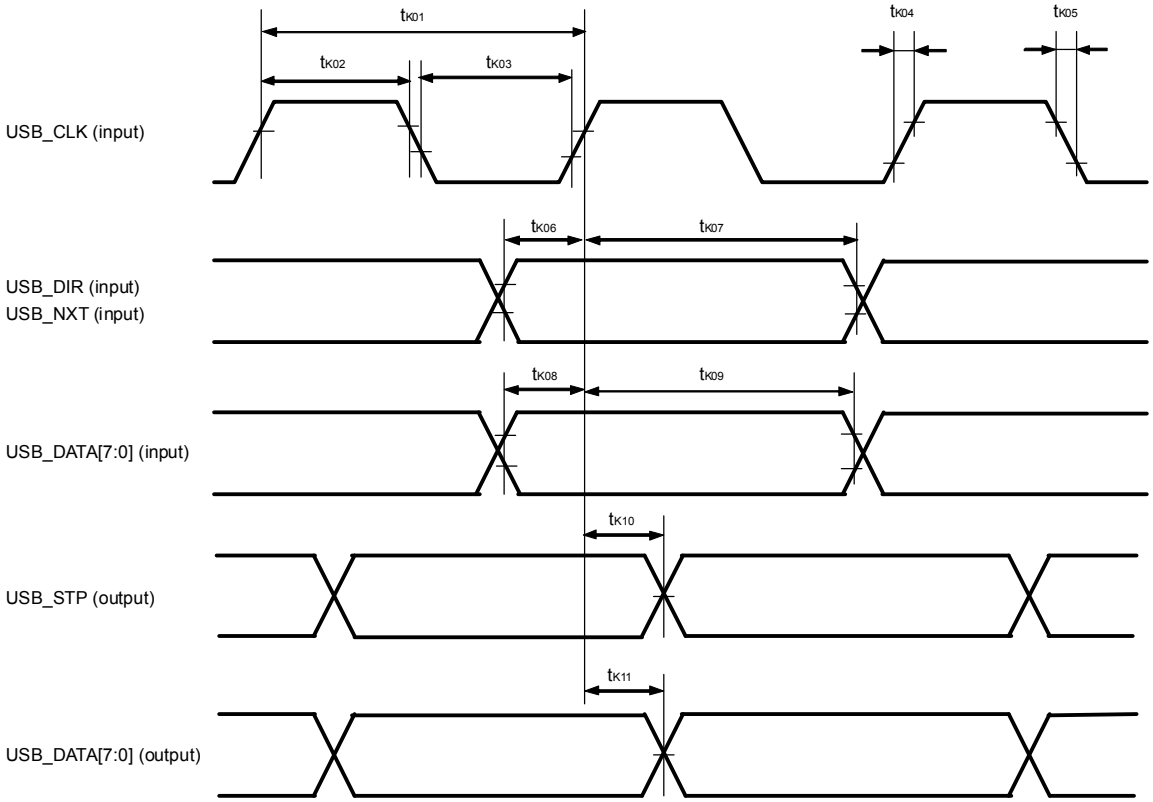
Figure 2-16. LCD Interface Timing



2.5.10 USB interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB_CLK cycle	t_{K01}	60 MHz	−	16.7	−	ns
USB_CLK high-level width	t_{K02}	−	7	−	−	ns
USB_CLK low-level width	t_{K03}	−	7	−	−	ns
USB_CLK rise time	t_{K04}	−	−	−	2	ns
USB_CLK fall time	t_{K05}	−	−	−	2	ns
USB control input setup time	t_{K06}	−	5	−	−	ns
USB control input hold time	t_{K07}	−	1	−	−	ns
USB data input setup time	t_{K08}	−	5	−	−	ns
USB data input hold time	t_{K09}	−	1	−	−	ns
USB data output delay time	t_{K11}	−	0.5	−	7	ns
USB_STP output delay time	t_{K10}	−	1	−	9	ns

Figure 2-17. USB Interface Timing

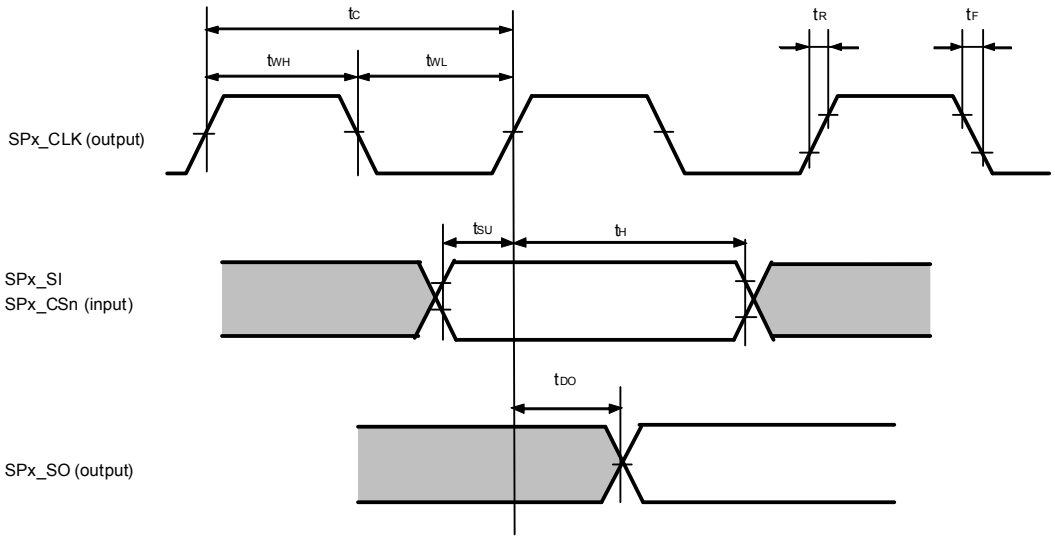


2.5.11 SPI interface

(1) Master mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common to SP0, SP1, and SP2						
SPx_CLK output cycle	t_C	−	40	−	−	ns
SPx_CLK high-level width	t_{WH}	−	16	−	−	ns
SPx_CLK low-level width	t_{WL}	−	16	−	−	ns
SPx_CLK rise time	t_R	20 to 80%		−	4	ns
SPx_CLK fall time	t_F	80 to 20%		−	4	ns
SP0						
SP0_SI setup time	t_{SU0}	Rising and falling edges of SP0_CLK	12	−	−	ns
SP0_SI hold time	t_{H0}	Rising and falling edges of SP0_CLK	0	−	−	ns
SP0_SO delay time	t_{DO0}	Rising and falling edges of SP0_CLK	0	−	12	ns
SP1						
SP1_SI setup time	t_{SU1}	Rising and falling edges of SP1_CLK	12	−	−	ns
SP1_SI hold time	t_{H1}	Rising and falling edges of SP1_CLK	0	−	−	ns
SP1_SO delay time	t_{DO1}	Rising and falling edges of SP1_CLK	0	−	12	ns
SP2						
SP2_SI setup time	t_{SU2}	Rising and falling edges of SP2_CLK	12	−	−	ns
SP2_SI hold time	t_{H2}	Rising and falling edges of SP2_CLK	0	−	−	ns
SP2_SO delay time	t_{DO2}	Rising and falling edges of SP2_CLK	0	−	12	ns

Figure 2-18. SPI Interface Timing (Master Mode)



Remarks 1. The level of the SPx_CLK output can be inverted by setting a register.

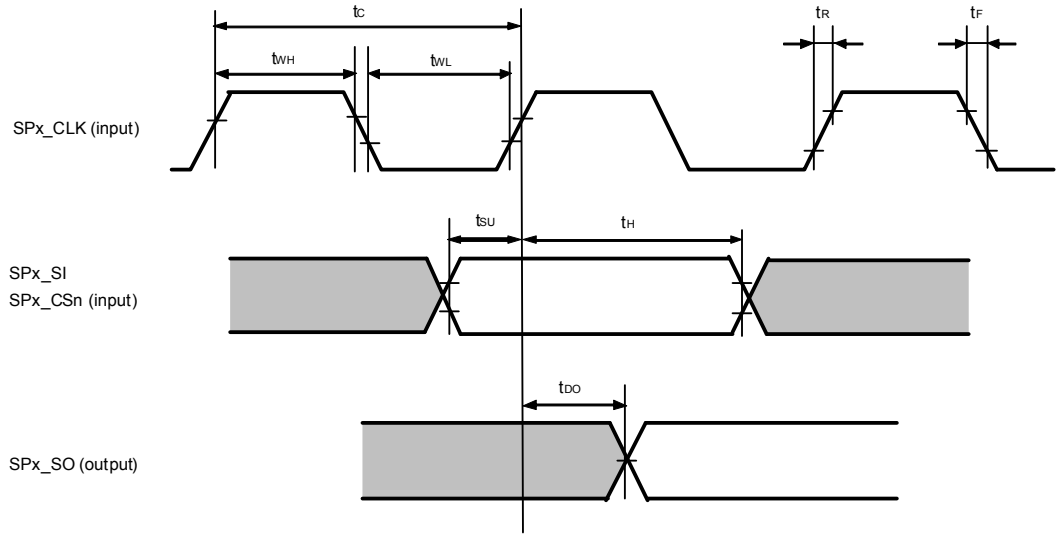
2. SPx_CLK is not output while SPx_CLK is inactive. (Fixed to inactive.)

3. If the read latency of the connected device is long, the time can be adjusted by means such as using a function to switch the I/O phase of SI and SO (by using the rise and fall of SCLK).

(2) Slave mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common to SP0, SP1, SP2						
SPx_CLK input cycle	t_C	–	50	–	–	ns
SPx_CLK high-level width	t_{WH}	–	20	–	–	ns
SPx_CLK low-level width	t_{WL}	–	20	–	–	ns
SPx_CLK rise time	t_R	–	–	–	4	ns
SPx_CLK fall time	t_F	–	–	–	4	ns
SP0						
SP0_CS setup time	t_{SU0}	Rising and falling edges of SP0_CLK	5	–	–	ns
SP0_CS hold time	t_{H0}	Rising and falling edges of SP0_CLK	15	–	–	ns
SP0_SO delay time	t_{DO0}	Rising and falling edges of SP0_CLK	3	–	18	ns
SP1						
SP1_CS setup time	t_{SU1}	Rising and falling edges of SP1_CLK	5	–	–	ns
SP1_CS hold time	t_{H1}	Rising and falling edges of SP1_CLK	15	–	–	ns
SP1_SO delay time	t_{DO1}	Rising and falling edges of SP1_CLK	3	–	20	ns
SP2						
SP2_CS setup time	t_{SU2}	Rising and falling edges of SP2_CLK	5	–	–	ns
SP2_CS hold time	t_{H2}	Rising and falling edges of SP2_CLK	15	–	–	ns
SP2_SO delay time	t_{DO2}	Rising and falling edges of SP2_CLK	3	–	18	ns

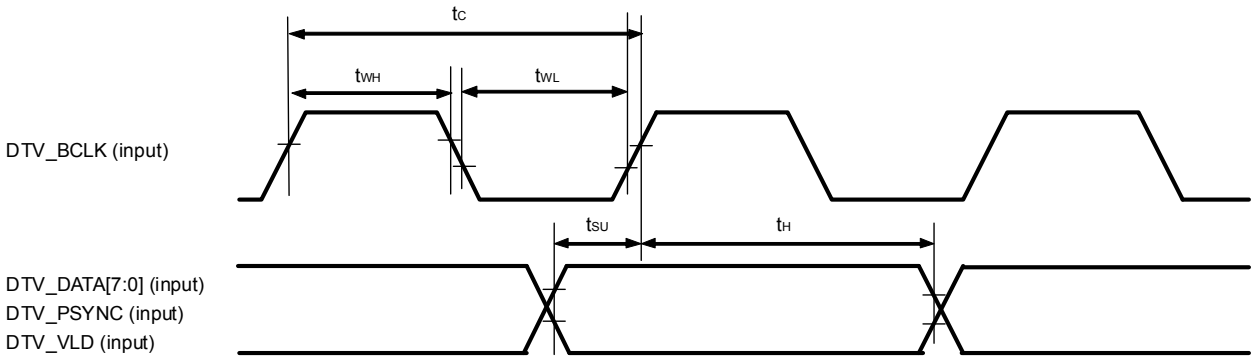
Figure 2-19. SPI Interface Timing (Slave Mode)



2.5.12 DTV interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DTV_BCLK input cycle	t_C	–	66	–	–	ns
DTV_BCLK high-level width	t_{WH}	–	28	–	–	ns
DTV_BCLK low-level width	t_{WL}	–	28	–	–	ns
DTV_DATA, DTV_PSYNC, DTV_VLD setup time	t_{SU}	–	12	–	–	ns
DTV_DATA, DTV_PSYNC, DTV_VLD hold time	t_H	–	12	–	–	ns

Figure 2-20. DTV Interface Timing



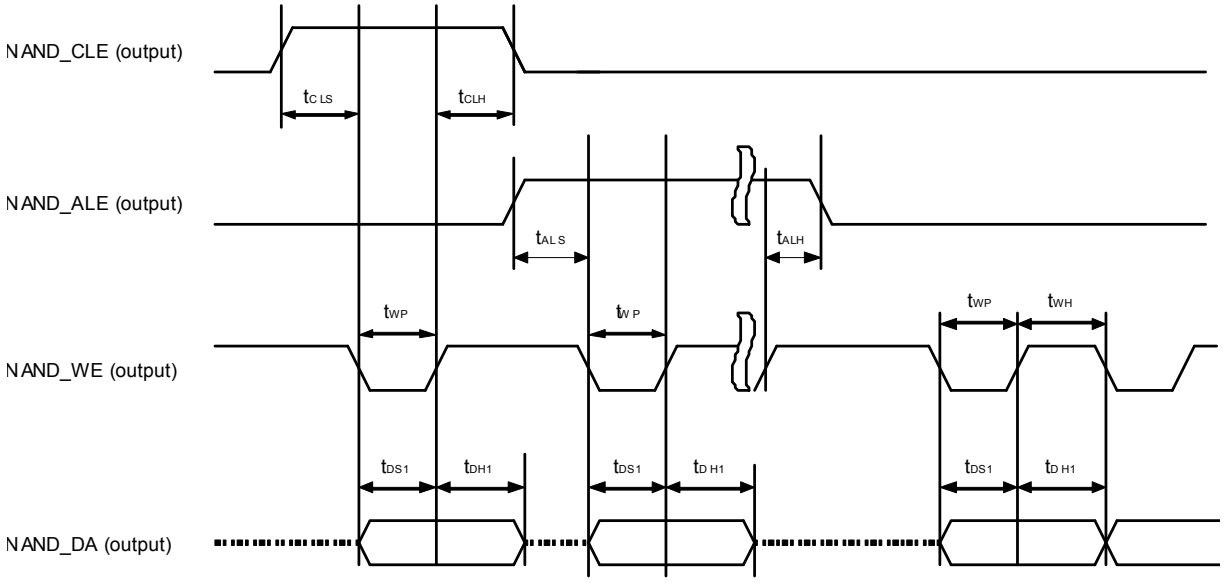
2.5.13 NAND Flash interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLE setup time	t_{CLS}	–	t_{C-3}	–	8 t_{C+3}	ns
CLE hold time	t_{CLH}	–	t_{C-3}	–	8 t_{C+3}	ns
ALE setup time	t_{ALS}	–	t_{C-3}	–	8 t_{C+3}	ns
ALE hold time	t_{ALH}	–	t_{C-3}	–	8 t_{C+3}	ns
Write pulse width	t_{WP}	–	t_{C-3}	–	16 t_{C+3}	ns
WEZ high-level hold time	t_{WH}	–	t_{C-3}	–	16 t_{C+3}	ns
Write data setup time	t_{DS1}	Rising edge of NAND_WEZ	t_{WP-3}	–	t_{WP+3}	ns
Write data hold time	t_{DH1}	Rising edge of NAND_WEZ	t_{WH-3}	–	t_{WH+3}	ns

Remarks 1. $t_C = t_{C\ (AHB)}$ in the above table

2. The AC characteristics for NAND_WEZ, REZ, CLE, and ALE are determined by a register setting, and the unit is t_C (when AHB = 83 MHz with ACPU operating at 500 MHz).

Figure 2-21. NAND Flash Interface Timing 1



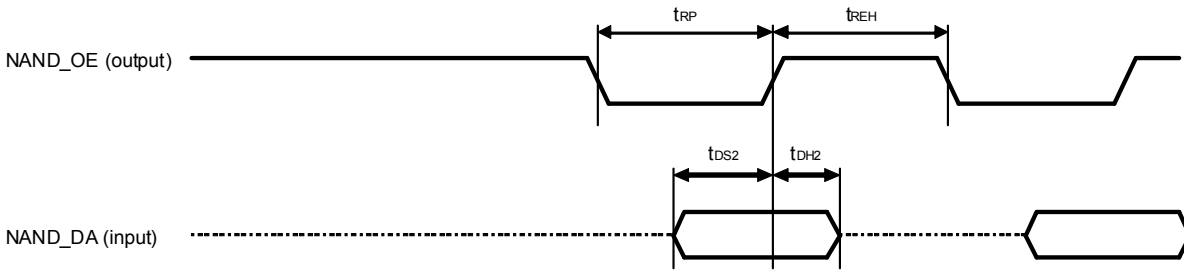
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Read pulse width	t_{RP}	–	t_{C-3}	–	16 t_{C+3}	ns
High-level hold time	t_{REH}	–	t_{C-3}	–	16 t_{C+3}	ns
Read data setup time	t_{DS2}	Rising edge of NAND_OE	8	–	–	ns
Read data hold time	t_{DH2}	Rising edge of NAND_OE	0	–	–	ns

Remarks 1. t_C in the above table = t_C when AHB = 83 MHz with ACPU operating at 500 MHz, = 12 ns

2. The AC characteristics for NAND_WE, OE, CLE, and ALE are determined by a register setting, and the unit is t_C.

3. The internal bus clock is used for data latching during reading via NAND_DA (input).

Figure 2-22. NAND Flash Interface Timing 2

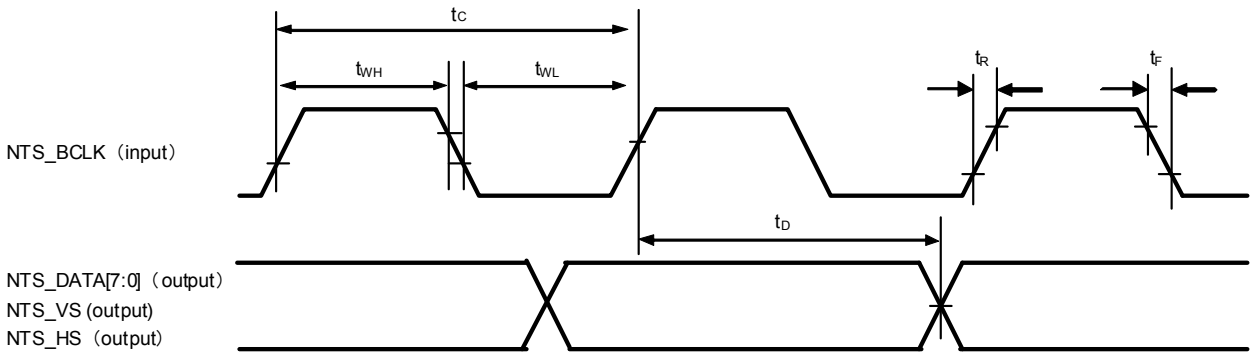


2.5.14 ITU-R BT.656 interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NTSC_CLK input cycle	t_C	–	–	37[Note]	–	ns
NTSC_CLK high-level width	t_{WH}	–	13	–	–	ns
NTSC_CLK low-level width	t_{WL}	–	13	–	–	ns
NTSC_CLK rise time	t_R	–		–	5	ns
NTSC_CLK fall time	t_F	–		–	5	ns
NTSC_DATA output delay time	t_D	Rising edge of NTSC_CLK	4	–	18	ns

Note NTSC_CLK = 27 MHz

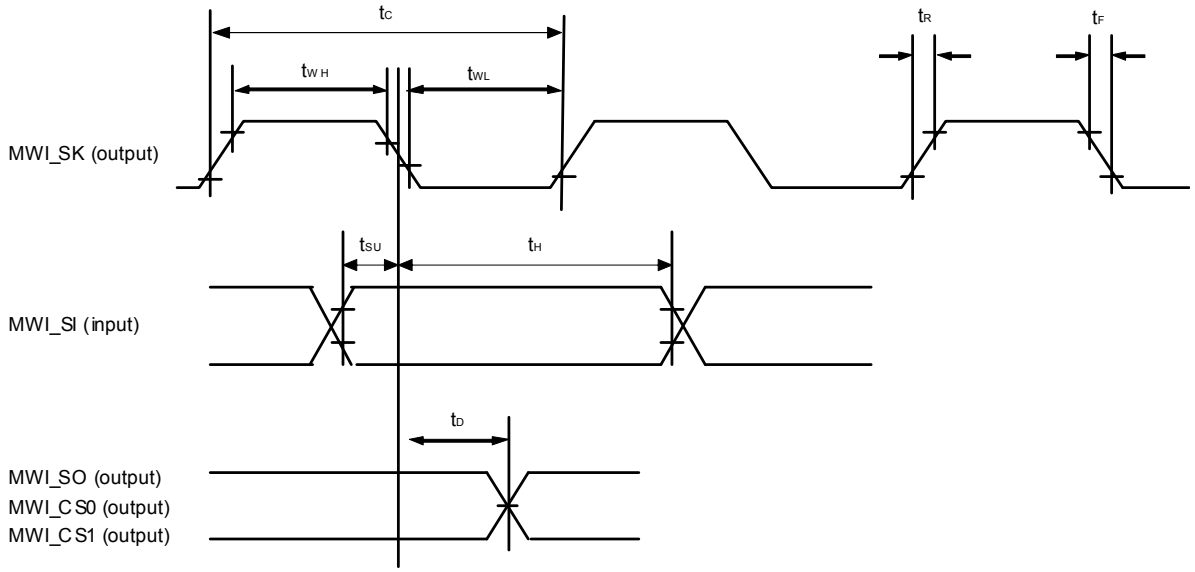
Figure 2-23. ITU-R BT.656 Interface Timing



2.5.15 MICROWIRE interface

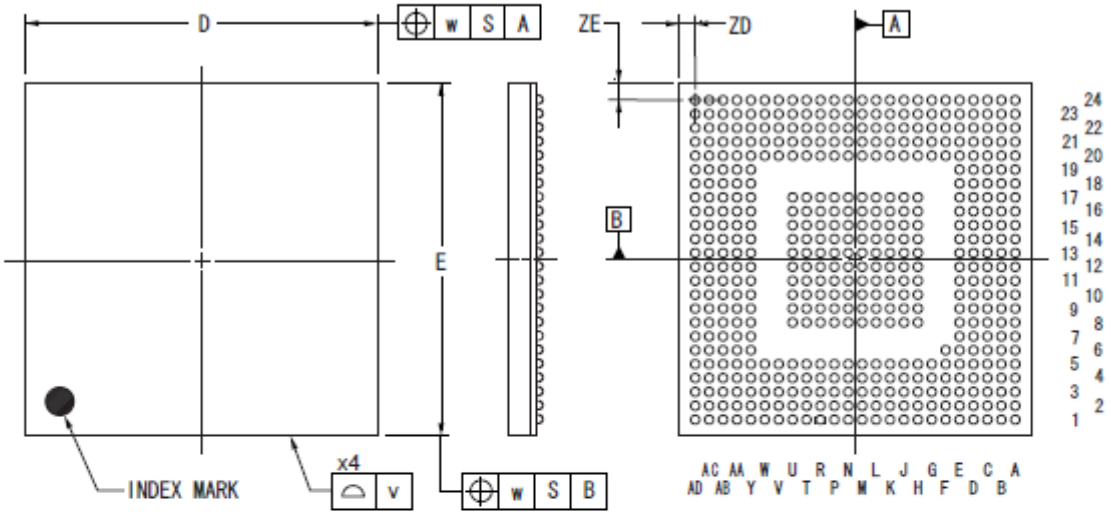
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MWI_SK clock cycle	t_C	–	160	–	–	ns
MWI_SK clock high-level width	t_{WH}	–	72	–	–	ns
MWI_SK clock low-level width	t_{WL}	–	72	–	–	ns
MWI_SK clock rise time	t_R	–	–	–	8	ns
MWI_SK clock fall time	t_F	–	–	–	8	ns
MWI_SI setup time	t_{SU}	Rising edge of MWI_SK	20	–	–	ns
MWI_SI hold time	t_H	Rising edge of MWI_SK	0	–	–	ns
MWI_SO, MWI_CSn output delay time	t_D	Rising edge of MWI_SK	–	–	20	ns

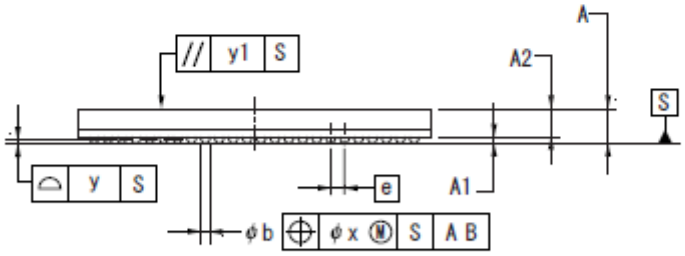
Figure 2-24. MICROWIRE Interface Timing



3. PACKAGE DRAWING

481-PIN PLASTIC FBGA(12.7x12.7)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.70±0.10
E	12.70±0.10
v	0.15
w	0.20
A	1.21±0.09
A1	0.21±0.05
A2	1.00
e	0.50
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P481F1-50-ENY

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..
June 30, 2009	3.0	Incremental update from comments to the 2.0. The item of the power supply start-up sequence is added. (chapter 2.5.16)
September 30, 2009	4.0	Incremental update from comments to the 3.0. UTEST pins : Handling When Not Used : Leave open -> “L” level hold. Power supply start-up (chapter 2.5.17) sequence is indicated on a user's manual (one chip).
December 22, 2009	5.0	Incremental update from comments to the 4.0. The specification of the self refresh current is changed with name of product change (MC-10118A->, MC-10118B).
February 15, 2010	6.0	Incremental update from comments to the 5.0. Change in the product name (MC-10118A/B->, MC-10118). A self-refresh electric current was returned to the value of revision 4.0.
March 31, 2010	7.0	Order name change (MC-10118AF1-ENY-A -> MC-10118BF1-ENY-A). The specification of the self refresh current is changed with name of product change (MC-10118->, MC-10118B).

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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